MT6260A GSM/GPRS/EDGE-RX SOC Processor Technical Brief

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read o ly. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) aut matic lly.
WO	Write only
W1S	Write o y. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding it.

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1 System Overview

MT6260A is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS p ocess

MT6260A is a featu e-rich and extremely powerful single-chip olution for high-end GSM/GPRS and EDGE-Rx capability. Based on the 32-bit ARM7EJ-S™ RISC processor, MT6260A's superb processing power, along with high bandwidth architecture and dedicated hardware support, provides a p atform for high-performance GPRS/EDGE-Rx Class 12 MODEM application and leading edge multimedia applications.

MT6260A also features:

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v3.0.
- A FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.

Typical application diagram is shown in Figure 1.

Platform

MT6260A is capable of running the ARM7EJ-S™ RISC processor, which provides the best trade-off between system performance and power consumption.

For large amounts of data transfer, high-performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing the MCU processing load.

Targeted as a media-rich platform for mobile applications, MT6260A also provides hardware security digital rights management for copyright protection. For further safeguard and to protect the manufacturer's development investment, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Memory

MT6260A supports serial flash interface with various operating frequencies.

Multimedia

The MT6260A multimedia subsystem provides conventional parallel interface and 2-bit serial interface for CMOS sensors. The camera resolution is up to 2M pixels. The software-based codec can be used to process various video types. Besides, MT6260A provides fancy UI capabilities through its hardware 2D accelerator. The 2D accelerator performs igh-speed linear transformations with filtering. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT6260A is implemented with a high-pe formance audio synthesis technology, as well as a high quality audio amplifier to provide superior audio experiences.

Connectivity and storage

MT6260A supports UART, USB 1.1 FS/LS , SDIO, HIF interface nd MMC/SD storage systems. These interfaces p ovide MT6260A users with the highest level of lexibility in implementing high-end solutions

To achieve a complete user interface, MT6260A also brings together all the necessary peripheral blocks for a multimedia GSM/GPRS/EDGE-RX phone. The peripheral blocks include the keypad scanner with the capability to detect multiple key

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presses, SIM controller, real-time clock, PWM, serial/parallel LCD controller and general-purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal audio front-end, the MT6260A architecture provides easy audio interfacing with direct connection to the audio transducers The audio interface integrates A/D converters for voice band, as well as high-resolution tereo D/A converters for both audio and voice band

MT6260A supports AMR codec to adaptively optimize the quality of speech a d audio. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit r tes.

In addition, a 1.2W audio amplifier is lso embedded to save the BOM cost of adopting external amplifiers.

GSM/GPRS/EDGE-Rx radio

MT6260A integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT6260A achieves outstanding MODEM performance by utilizing a highly dynamic range ADC in the RF downlink path.

MT6260A embeds a high-performance and completely integrated single-ended SAW-less RF transceiver for multi-band GSM cellular system. In this RF transceiver, a quad-band receiving feature with high sensitivity is supported utilizing one RF receiver and a fully integrated channel filter. With ultra-high dynamic range, the off-chip balun and SAW filters on the receiving path can be removed for BOM cost reduction. In addition, the minimum component count is guaranteed by realizing a highly integrated transmitter, low-spur frequency synthesizer and a Digitally-Controlled Crystal Oscillator (DCXO).

Bluetooth radio

MT6260A offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components are required. MT6260A provides superior sensitivity and class 1 output power and thus ensures the quality of the connection with a wide range of Bluetooth devices.

MT6260A is fully compliant with Bluetooth v3.0 and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with 802.11 system.

MT6260A supports rich Bluetooth profiles, enabling diversified applications that are widely used on the handset with excellent interoperability.

FM radio

The FM adio subsystem provides a completely integrated FM Rx receiver supporting 87.5 ~ 108MHz FM bands with 50kHz tuning step. It also performs fast channel seek/scan algorithm to validate 200 carrier frequencies in 6 seconds. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve ex ellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize Rx system performance in all ranges of signal quality by reference of a very sophisticated channel quality index (CQI). When the received signal quality is poor, the design not

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only enhances the ACI rejection capability but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.

The FM radio subsystem supports both long antenna, which s usually an earphone, and auto-calibrated sh rt antenna, which is usually a FPC short antenna o shared antenna with GSM for different app cation scenarios.

Debugging function

The JTAG interface enables in-circuit debugging of the software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT6260A provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power management

A power management is embedded in MT6260A to provide rich features a high-end feature phone supports, including Li-ion battery charger, high performance and low quiescent current LDOs, and drivers for LED and backlight.

MT6260A offers various low-power features to help reduce the system power consumption. MT6260A is also fabricated in an advanced low-power CMOS process, hence providing an overall ultra-low leakage solution.

Package

The MT6260A device is offered in a 9.6mm×8.6mm, 199-ball, 0.5mm pitch, TFBGA package.

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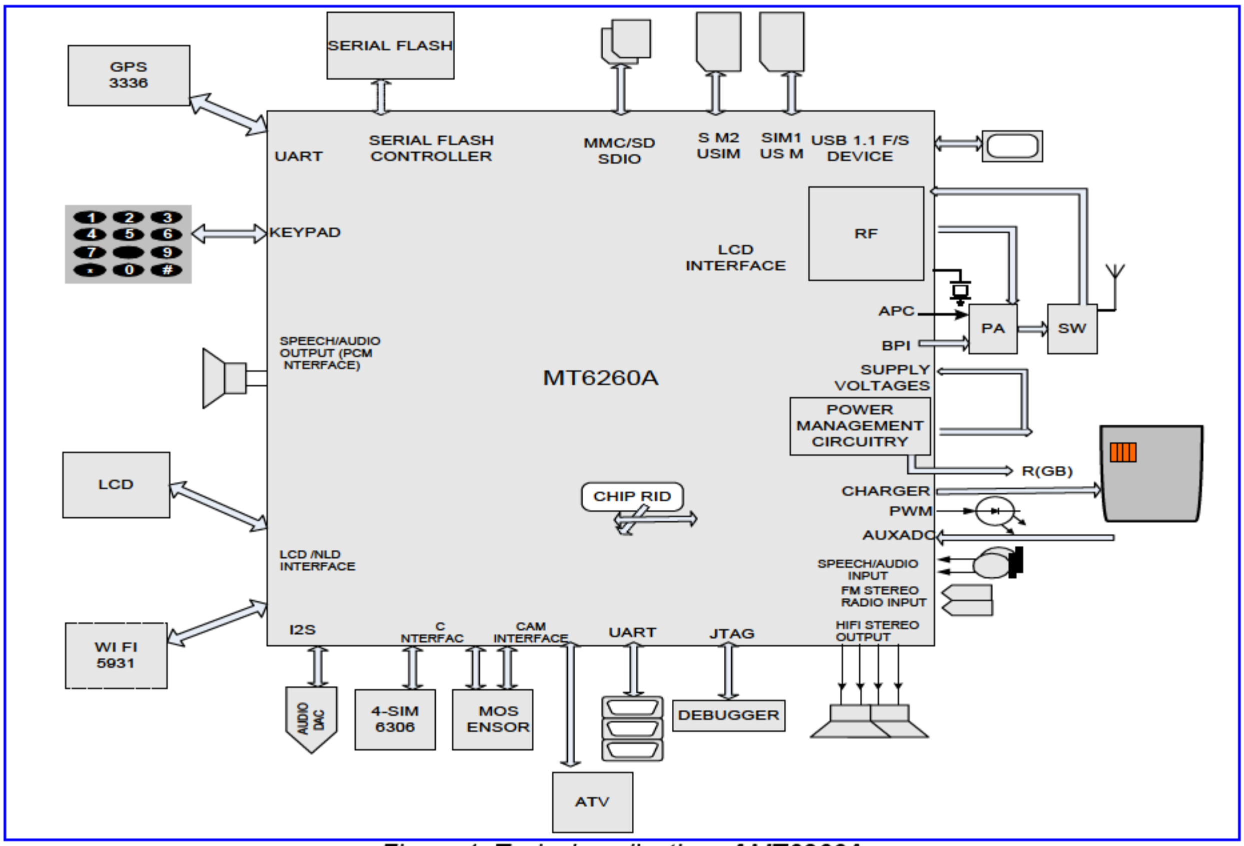

Figure 1. Typical application of MT6260A

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1.1 Platform Features

General

- Integrated voi e-band, audio-band and base-band analog front-end
- Integrated f ll-fe tured power management unit

MCU subsystem

- ARM7EJ-S™ 32-bit RISC processor
- Java hardware acceleration for fast Java-based games and applets
- High-performance multi-layer AHB bus
- Dedicated DMA bus with 15 DMA channels
- On-chip boot ROM for factory fla h programming
- Watchdog timer for system crash recov ry
- 4 sets of general-purpose timers
- Circuit switch data coprocessor
- Division coprocessor

Serial flash interfaces

- Supports various operating frequency combinations for serial flash
- Supports QPI and SPI serial flash

User interfaces

- 5-row x 5-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- Dual SIM/USIM controller with hardware T = 0/T = 1 protocol control
- Real-time clock (RTC) operating with a low-quiescent-current power supply
- General-purpose I/Os (GPIOs) available for auxiliary applications
- 1 sets of Pulse Width Modulation (PWM) output
- 16 external interrupt lines
- 1 external channel auxiliary 10-bit A/D converter

Security

- Supports security key and chip random ID

Connectivity

- 2 UARTs with hardware flow control and supports baud rate up to 921,600 bps
- FS/LS USB 1.1 device controller
- Multimedia card, secure digital Memory Card, host controller with flexible I/O voltage power
- Supports SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for audio applications

  I2C master interface for peripheral management including image sensors
- SPI master interface for peripheral mana ement.

Power management

- Li-ion battery charger
- 14 LDOs fo the power supply of memory card, camera, Bluetooth, RF, SIM card and other diversified usage
- 4 open-drain outpu switches to supply/control the LED
- LDO type vibrato
- One NMOS switch to control keypad LED
- Thermal overload protection
- Under-voltage lock-out prot ction
- Over-voltage protection
- Different levels of sleep modes with sophisticated software control enables excellent power saving performance.

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Test and debugging

- Built-in digital and analog loop back modes for both audio and baseband front-end
- DAI port complies with GSM Rec.11.10.
- JTAG port for debugging embedded MCU

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1.2 MODEM Features

Radio interface and baseband front-end

- Digital PM dat path with baseband front-end
- High dyn mic range delta-sigma ADC converts the dow link analog I and Q signals to digital baseband
- 10-bit D/A converter for Automatic Power Control (APC)
- Programmable radio Rx filter with adaptive gain control
- Dedicated Rx filter for FB acquisition
- 4-pin Baseband Parallel Interface (BPI) with programmable driving strength
- Supports multi-band

Voice and modem CODEC

- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression
- Advanced sidetone oscillation reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- Supports GSM/GPRS/EDGE-Rx modem
- GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS/EDGE-Rx GEA1, GEA2 and GEA3 ciphering
- GPRS packet switched data with CS1/CS2/CS3/CS4 coding schemes
- EDGE-Rx with MCS1-9 receiver coding schemes
- GSM circuit switch data
- GPRS/EDGE-Rx Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS(Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec.

Voice interface and voice front-end

- Two microphone inputs share one low-noise amplifier with programmable gain and Automatic Gain Control (AGC) mechanisms
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D converter for voice uplink path
- Shares D/A converter with audio playback path
- Supports full-duplex hands-free operation
- Compliant with GSM 03.50

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1.3 GSM/GPRS/EDGE RF Features

Receiver

- Dual single-ended input LNAs support Quad bandQua ratur RF mixer
- Fully integrated hannel filter
- High dynam c ange ADC
- 12dB PGA gain with 6dB gain step

Transmitter

- Transmitter outputs suppo t quad bands.
- Highly precise and low noise RF transmitter for GSM/GPRS applications

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GPRS/EDGE-Rx applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Low power mode supports 32K crystal removal

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1.4 Multimedia Features

LCD/ WiFi inte face

- Dedicated pa allel interface supports 3 external device with 8-bit for WiFi interface and 8-/9-bit or p allel LCD interface.

LCD controller

- Supports simultaneous connection to 2 parallel and 2 serial LCD modules
- LCM formats supported: RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 480x320
- Per pixel alpha channel
- True color engine
- Supports hardware display rotation
- Capable of combining display memories with up to 4 blending layers

Camera interface

- YUV422 format image input
- Capable of processing image of size up to 0.3M pixels (Mediatek serial interface) and 2M pixels (w/o compression)

JPEG decoder

- Baseline JPEG decoding
- Supports various YUV formats, DC/AC Huffman tables and quantization tables

JPEG encoder

- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 compliance
- Supports YUV420 and grayscale formats
- Supports EXIF/JFIF
- Standard DC and AC Huffman tables
- Provides 5 levels of encode quality
- Supports zeros shutter delay

MJPEG

- Decode spec: HVGA@10fps
- Encode spec: HVGA@10fps

Image data processing

- Supports 4x digital zoom
- High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.
- Horizontal scaling with bilinear interpolation
- Vertical scaling with bilinear interpolation
- YUV and RGB color space conversion
- RGB/YCbCr format thumbnail output

MPEG-4/H.263 CODEC

- Software-based MPEG4 encoder
- Software-based MPEG4 decoder
- ISO/IEC 14496-2 simple profile:
  - Decode spec: HVGA@25fps
  - Encode spec: QVGA@15fps
- ISO/IEC 14496-2 advanced simple profile:
  - Decode @ level 0/1/2/3
  - ITU-T H.263 profile 0 @ level 40
- Supp rts visual tools for decoder: I-VOP, P VOP, B-VOP, AC/DC prediction, 4-MV, unrestri ted MV, error resilience, short header, global motion compensation, method 1/2 quantization, quarter-pel motion compensation.
- Error resilience for decoder: Slice resynchronization, data partitioning, reversible VLC
- Supports vis al tools for encoder: I-VOP, P-VOP, Half-Pel, DC prediction, unrestricted MV, short heade

H.264

- ISO/IEC 14496-10 baseline p ofile
  - Decode spec: QVGA@20fps

2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, 24-bpp ARGB6666.

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- 4 layers overlay with individual color format, window size, source key, constant alpha and rotation
- Rectangle fill with constant
- BitBlt: Capable with 7 rotation types
- Alpha blending with 7 rotation types, per-pixel al ha and pre-multiplied alpha
- Font drawing Normal font and anti-aliasing font
- Linear trans ormation: Supports perspective transform, tru cate/nearest/bi-linear sample filter.

Audio CODEC

- Supports AAC codec decoding
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set o 128 instruments and 47 sets of percussions
- PCM playback and record
- Digital audio playback

Audio interface and audio front-end

- Supports I2S interface
- High-resolution D/A converters for stereo audio playback
- Voice band A/D converter support
- Stereo to mono conversion

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1.5 Bluetooth Features

Radio features

- Fully complian with Bluetooth specification 3.0 + EDR
- Low out-of- and spurious emissions support simultaneou opera ion with GPS and GSM/GPRS worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 10dBm output power
- -95dBm sensitivity with excelle t interference rejection performanc
- Hardware AGC dynamically adjusts receiver performance in changing environments

Baseband features

- Up to 4 simultaneous active ACL links
- Up to 1 simultaneous SCO or eSCO link with CVSD coding
- Supports eSCO
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan
- Supports sniff mode
- AFH and PTA collaborative support for WLAN/BT coexistence
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption
- Channel quality driven data rate adaptation
- Channel assessment for AFH

Platform features

- Embedded processor for Bluetooth protocol stack with built-in memory system
- Fully verified ROM based system with code patch for feature enhancement

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1.6 FM Features

- 76-108MHz worldwide FM bands with 50kHz tuning step
- Supports RDS/RBDS radio data system
- Supports lo g/short antenna
- 40ms seek time per channel, and 9sec search time for all channels (87.5 ~ 108MHz)
- Superior stereo noise reduction
- Soft mute volume control
- Supports short antenna, auto calibration for different FM channels
- 60dB SINAD with 22.5kHz FM deviation
- 3dBuVemf FM RX sensitivity w th superior interference rejection
- 20dBuVemf RDS sensitivity (dev: 2kHz)
- More than 55dBc rejection capability again t -200kHz ACI

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1.7 General Descriptions

Figure 2 is the block diagram of MT6260A. Based on a multi- rocessor architecture, MT6260A integrates an ARM7EJ-S™ core, the main processor unni g high-level GSM/EDGE-Rx protoco software as well as multimedia applications, single digital signal processor core, which manages the low-level MODEM and advanced audio functions, an embedded processor running Bluetooth baseband and link control pr tocol and the Bluetooth radio control.

MT6260A consists of the following subsystems:

- Microcontroller Unit (MCU) subsystem: Includes an ARM7EJ-S™ RISC processor and its accompanying memory management and interrupt handling logics
- Digital Signal Processor (DSP) subsystem: Includes a DSP and its accompanying memory, memory controller and interrupt controller
- MCU/DSP interface: Junction at which the MCU and the DSP exchange hardware and software information
- Microcontroller peripherals: Include all user interface modules and RF control interface modules
- Microcontroller coprocessors: Run computing-intensive processes in place of the microcontroller
- DSP peripherals: Hardware accelerators for GSM/GPRS/EDGE-Rx channel codec
- Multimedia subsystem: Integrates several advanced accelerators to support multimedia applications
- Voice front-end: Data path for converting analog speech to and from digital speech
- Audio front-end: Data path for converting stereo audio from an audio source
- Baseband front-end: Data path for converting a digital signal to and from an analog signal from the RF modules
- Timing generator: Generates the control signals related to the TDMA frame timing
- Power, reset and clock subsystem: Manage the power, reset and clock distribution inside MT6260A.
- Bluetooth subsystem: Includes an embedded processor with embedded ROM/RAM system, baseband processor, and a high-performance radio block
- Power management unit: Self-contained power supply source which also controls the charging and system startup circuitry.

De ails of the individual subsystems and blocks are descr bed in the following chapters.

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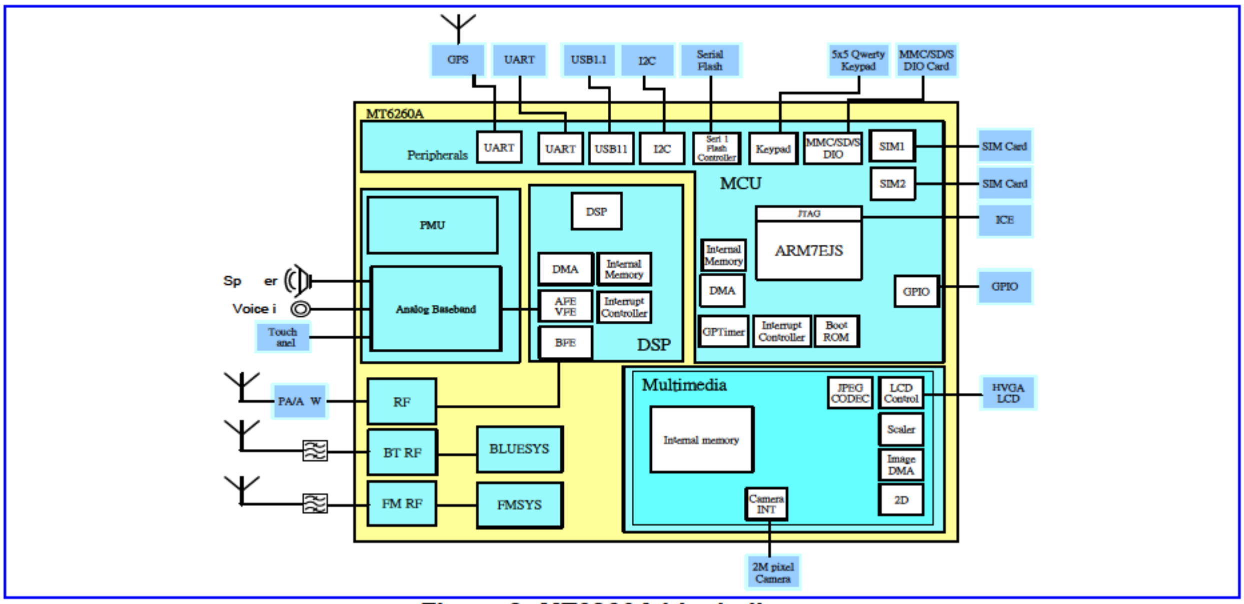

Figure 2. MT6260A block diagram

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2 Product Descriptions

2.1 Pin Description

2.1.1 Ball Diagram

For MT6260, an TFBGA 9.6mm*8.6mm, 199-ball, 0.5mm pitch package is offered. Pin-outs and the top view are illu trate in **Figure 3** for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	AVSS_2G	RXLB_P	RXLB_N		AVSS_2G	XTAL1			DVDD28		URXD2	CMPCLK		CMPDN	CMDAT5		CMMCLK	KCOL1	GND	A
B	RXHB_P	RXHB_N		TP2	TP4	XTAL2	AVSS_BT	BT_LNA	DVDD28_FSRC	UTXD1	UTXD2	CMRST	CMDAT3	CMDAT0	CMDAT4	CMVREF	GPIO19	GPIO17	GPIO16	B
C	TXO_LB	TXO_HB	AVSS_2G	TP1	TP3		CLK_SEL	AVSS_BT	BPI_BUS1	BPI_BUS0	URXD1		CMDAT2	KROW1	CMDAT7	KROW2	KROW0	KCOL4	EDICK	C
D	AVSS_2G	AVSS_2G		AVSS_2G		FREF1			BPI_BUS2		BPI_BUS3	CMDAT6		DVDD28		SCL28	KROW4	KROW3	EDIWS	D
E	VCAMA	VRF	VBAT_VA		AVSS43_PMU		AVSS_2G				CMHREF	CMDAT1					KCOL0	KCOL2		E
F		VCAMD		VREF		BATSNS			AVDD28_2GAFE	VDDK				DVDD18_EMI	DVDD18_EMI	WATCHDOG	KCOL3	SDA28	EDIDAT	F
G		ISINK0	ISINK1	TESTMODE	AGND	ISENSE				GND		GND				NLD1	NLD0		GND	G
H	KPLED	ISINK2	ISINK3	PWRKEY							GND					NLD7	NLD2	LSRSTB		H
J	DRV	BATDET	CHR_LDO	VCDT		BATON	AVSS43_PMU		SRCLKENAI	GND		GND				LSCE1_B	LPTE	NLD3	NLD8	J
K	FLYN	FLYP		AVSS43_CP			AVSS43_PMU		XTAL_SEL	RESETB		VDDK				LPA0	NLD4	LPRSTB	NLD6	K
L		VBOOST	AVDD43_CP	AVSS43_SPK	AVSS43_PMU			VRTC	XIN	XOUT						LWR_B	LRD_B	LPCE0_B		L
M	SPK_OUTP	SPK_OUTN	VBAT_SPK			AVSS43_PMU										DVDD28_SF	LPCE1_B	GND	GND	M
N			ACCDET					VUSB	VSIM2	VSIM1						SCK	SWP	NLD5		N
P	APC	AU_MICBIAS1			HSP												SHOLD	SFCS0	MCINS	P
R	AUX_IN4	AU_MICBIAS0	XP		HSN		VSF	VMC						SIM1_SIO	SIM2_SIO	DVDD33_MSDC	MCDA3	SFCS1	SIN	R
T	AU_VIN0_P	AU_VIN1_N	YP	XM	HPL	VIBR		VIO18	VCORE	AVSS_FM	FM_ANT_N	AVDD28_FM	USB11_DP	SIM1_SRST	SIM2_SRST	MCDA0	MCCM0	MCDA1	SOUT	T
U	AU_VIN0_N	AU_VIN1_P	YM	AVSS28_ABB	HPR	VA		VIO28	VBAT_DIGITAL		FM_ANT_P	GND	USB11_DM	SIM1_SCLK		SIM2_SCLK	MCDA2	MCCK	GND	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Figure 3. ***Ball diagram and top view***

2.1.2 Pin Coordination

Table 1. Pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	AVSS_2G	E5	AVSS43_PMU	M17	LPCE1_B
A11	URXD2	E7	AVSS_2G	M18	GND
A12	CMPCLK	F10	VDDK	M19	GND
A14	CMPDN	F14	DVDD18_EMI	M2	SPK_OUTN
A15	CMDAT5	F15	DVDD18_EMI	M3	VBAT_SPK
A17	CMMCLK	F16	WATCHDOG	M6	AVSS43_PMU
A18	KCOL1	F17	KCOL3	N10	VSIM1

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Pin#	Net name	Pin#	Net name	Pin#	Net name
A19	GND	F18	SDA28	N16	SCK
A2	RXLB_P	F19	EDIDAT	N17	SWP
A3	RXLB_N	F2	VCAMD	N18	NLD5
A5	AVSS_2G	F4	VREF	N3	ACCDET
A6	XTAL1	F6	BATSNS	N8	VUSB
A9	DVDD28	F9	AVDD28_2GAFE	N9	VSIM2
B1	RXHB_P	G10	GND	P1	APC
B10	UTXD1	G12	GND	P17	SHOLD
B11	UTXD2	G16	NLD1	P18	SFCS0
B12	CMRST	G17	NLD0	P19	MCINS
B13	CMDAT3	G19	GND	P2	AU_MICBIAS1
B14	CMDAT0	G2	ISINK0	P5	HSP
B15	CMDAT4	G3	ISINK1	R1	AUX_IN4
B16	CMVREF	G4	TESTMODE	R14	SIM1_SIO
B17	GPIO19	G5	AGND	R15	SIM2_SIO
B18	GPIO17	G6	ISENSE	R16	DVDD33_MSDC
B19	GPIO16	H1	KPLED	R17	MCDA3
B2	RXHB_N	H11	GND	R18	SFCS1
B4	TP2	H16	NLD7	R19	SIN
B5	TP4	H17	NLD2	R2	AU_MICBIAS0
B6	XTAL2	H18	LSRSTB	R3	XP
B7	AVSS_BT	H2	ISINK2	R5	HSN
B8	BT_LNA	H3	ISINK3	R7	VSF
B9	DVDD28_FSRC	H4	PWRKEY	R8	VMC
C1	TXO_LB	J1	DRV	T1	AU_VIN0_P
C10	BPI_BUS0	J10	GND	T10	AVSS_FM
C11	URXD1	J12	GND	T11	FM_ANT_N
C13	CMDAT2	J16	LSCE1_B	T12	AVDD28_FM
C14	KROW1	J17	LPTE	T13	USB11_DP
C15	CMDAT7	J18	NLD3	T14	SIM1_SRST
C16	KROW2	J19	NLD8	T15	SIM2_SRST
C17	KROW0	J2	BATDET	T16	MCDA0
C18	KCOL4	J3	CHR_LDO	T17	MCCM0
C19	EDICK	J4	VCDT	T18	MCDA1
C2	TXO_HB	J6	BATON	T19	SOUT
C3	AVSS_2G	J7	AVSS43_PMU	T2	AU_VIN1_N
C4	TP1	J9	SRCLKENAI	T3	YP
C5	TP3	K1	FLYN	T4	XM
C7	CLK_SEL	K10	RESETB	T5	HPL
C8	AVSS_BT	K12	VDDK	T6	VIBR
C9	BPI_BUS1	K16	LPA0	T8	VIO18
D1	AVSS_2G	K17	NLD4	T9	VCORE
D11	BPI_BUS3	K18	LPRSTB	U1	AU_VIN0_N
D12	CMDAT6	K19	NLD6	U11	FM_ANT_P

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Pin#	Net name	Pin#	Net name	Pin#	Net name
D14	DVDD28	K2	FLYP	U12	GND
D16	SCL28	K4	AVSS43_CP	U13	USB11_DM
D17	KROW4	K7	AVSS43_PMU	U14	SIM1_SCLK
D18	KROW3	K9	XTAL_SEL	U16	SIM2_SCLK
D19	EDIWS	L10	XOUT	U17	MCDA2
D2	AVSS_2G	L16	LWR_B	U18	MCCK
D4	A SS_2G	L17	LRD_B	U19	GND
D6	FREF1	L18	LPCE0_B	U2	AU_VIN1_P
D9	BPI_BUS2	L2	VBOOST	U3	YM
E1	VCAMA	L3	AVDD43 CP	U4	AVSS28 ABB
E11	CMHREF	L4	AVSS43_SPK	U5	HPR
E12	CMDAT1	L5	AVSS43_PMU	U6	VA
E17	KCOL0	L8	VRTC	U8	VIO28
E18	KCOL2	L9	XIN	U9	VBAT_DIGITAL
E2	VRF	M1	SPK OUTP		
E3	VBAT_VA	M16	DVDD28_SF		

2.1.3 Detailed Pin Description

Table 2. A ronym for pin types

Abbreviation	Description
AI	Analog input
AO	Ana og output
AIO	Analog bi-d ection
DI	Digital input
DO	Digital output
DIO	Digital bi direction
P	Power
G	Ground

Table 3. PIN function description and power domain

Pin name	Type	Description	Power domain
System			
RESETB	DIO	System reset	DVDD18_EMI
SRCLKENAI	DIO	26MHz clock request by external devices	DVDD18_EMI
GPIO16	DIO	General purpose input /output 16	DVDD28
GPIO17	DIO	General purpose input /output 17	DVDD28

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Pin name	Type	Description	Power domain
GPIO19	DIO	General purpose input /output 19	DVDD28
EDI interface			
EDICK	DIO	I2S clock	DVDD28
EDIDAT	DIO	I2S data	DVDD28
EDIWS	DIO	I2S word sync	DVDD28
RF control ci cuitro			
BPI_BUS0	DIO	RF hard-wire control bus bit 0	DVDD28
BPI_BUS1	DIO	RF hard-wire control bus bit 1	DVDD28
BPI_BUS2	DIO	RF hard-wire control bus bit 2	DVDD28
BPI_BUS3	DIO	RF hard-wire control bus bit 3	DVDD28
UART interface			
URXD1	DIO	UART1 receive data	DVDD28
UTXD1	DIO	UART1 transmit data	DVDD28
URXD2	DIO	UART2 receive data	DVDD28
UTXD2	DIO	UART2 transmit data	DVDD28
Keypad interface			
KCOL0	DIO	Keypad column 0	DVDD28
KCOL1	DIO	K ypad column 1	DVDD28
KCOL2	DIO	Key ad column 2	DVDD28
KCOL3	DIO	Keypad column 3	DVDD28
KCOL4	DIO	Keypad olumn 4	DVDD28
KROW0	DIO	Keypad row 0	DVDD28
KROW1	DIO	Keypad row 1	DVDD28
KROW2	DIO	Keypad row 2	DVDD28
KROW3	DIO	Keypad row 3	DVDD28
KROW4	DIO	Keypad row 4	DVDD28
Camera interface			
CMRST	DIO	CMOS sensor reset signal output	DVDD28
CMPDN	DIO	CMOS sensor power down c ntrol	DVDD28
CMVREF	DIO	CMOS sensor vertical reference signal input	DVDD28
CMHREF	DIO	CMOS sensor horizontal reference signal input	DVDD28
CMDAT0	DIO	CMOS sensor data input 0	DVDD28
CMDAT1	DIO	CMOS sensor data input 1	DVDD28
CMDAT2	DIO	CMOS sensor data input 2	DVDD28
CMDAT3	DIO	CMOS sensor data input 3	DVDD28
CMDAT4	DIO	CMOS sensor data input 4	DVDD28
CMDAT5	DIO	CMOS sensor data input 5	DVDD28
CMDAT6	DIO	CMOS sensor data input 6	DVDD28

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Pin name	Type	Description	Power domain
CMDAT7	DIO	CMOS sensor data input 7	DVDD28
CMPCLK	DIO	CMOS sensor pixel clock output	DVDD28
CMMCLK	DIO	CMOS sensor pixel clock input	DVDD28
MS/SD card interface			
MCINS	DIO	SD card detect Input	DVDD18_EMI
MCDA0	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCDA1	DIO	SD serial data IO 1/memory stick serial data IO	DVDD33_MSDC
MCDA2	DIO	SD serial data IO 2/memory stick serial data IO	DVDD33_MSDC
MCDA3	DIO	SD serial data IO 3/memory stick serial data IO	DVDD33_MSDC
MCCK	DIO	SD serial clock/memory stick serial clock	DVDD33_MSDC
MCCM0	DIO	SD command output/memory stick bus state output	DVDD33_MSDC
SIM card interface			
SIM1_SIO	DIO	SIM1 data input/outputs	VSIM1
SIM1_SRST	DIO	SIM1 card reset output	VSIM1
SIM1_SCLK	DIO	SIM1 card clock output	VSIM1
SIM2_SIO	DIO	SIM2 data inp t/outputs	VSIM2
SIM2_SRST	DIO	SIM2 card reset output	VSIM2
SIM2_SCLK	DIO	SIM2 card c ock utput	VSIM2
I2C interface			
SCL28	DIO	I2C clock 2.8v power domain	DVDD28
SDA28	DIO	I2C data 2.8v power domain	DVDD28
LCD interface			
LSRSTB	DIO	Serial display interface reset signal	DVDD18_EMI
LSCE1_B	DIO	Serial display interface chip select 1 output	DVDD18_EMI
LPCE1_B	DIO	Parallel display interface chip select 1 output	DVDD18_EMI
LPCE0_B	DIO	Parallel display interface chip select 0 output	DVDD18_EMI
LPTE	DIO	Parallel display interface tearing effect	DVDD18_EMI
LPRSTB	DIO	Parallel display interface reset signal	DVDD18_EMI
LRD_B	DIO	Parallel display interface read strobe	DVDD18_EMI
LPA0	DIO	Parallel display interface address output	DVDD18_EMI
LWR_B	DIO	Parallel display interface write strobe	DVDD18_EMI
NLD8	DIO	Parallel LCD data 8	DVDD18_EMI

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Pin name	Type	Description	Power domain
NLD7	DIO	Parallel LCD data 7	DVDD18_EMI
NLD6	DIO	Parallel LCD data 6	DVDD18_EMI
NLD5	DIO	Parallel LCD data 5	DVDD18_EMI
NLD4	DIO	Parallel LCD data 4	DVDD18_EMI
NLD3	DIO	Parallel LCD data 3	DVDD18_EMI
NLD2	DIO	Parallel LCD data 2	DVDD18_EMI
NLD1	DIO	Parallel LCD data 1	DVDD18_EMI
NLD0	DIO	Parallel LCD data 0	DVDD18_EMI
Watchdog reset			
WATCHDOG	DIO	Reset external memory device	DVDD18_EMI
General purpose I/O interface			
SFCS1	DIO	Serial Flash chip select 1	DVDD28_SF
SFCS0	DIO	Serial Flash chip select 0	DVDD28_SF
SIN	DIO	Serial Flash data input	DVDD28_SF
SOUT	DIO	Serial Flash data output	DVDD28_SF
SHOLD	DIO	Serial Flash data hold	DVDD28_SF
SWP	DIO	Seri l Flash write protect	DVDD28_SF
SCK	DIO	S rial Flash clock	DVDD28_SF
FM			
FM_ANT_P	AI	FM input from antenna	AVDD28_FM
FM_ANT_N	AI	FM input from antenna	AVDD28_FM
Bluetooth			
BT_LNA	AIO	Bluetooth RF single-end d input	DVDD28
2G RF			
RXHB_P	AI	RF input for highband Rx (DCS/PCS)	VRF
RXHB_N	AI	RF input for highband Rx (DCS/PCS)	VRF
RXLB_P	AI	RF input for lowband Rx (GSM900/GSM850)	VRF
RXLB_N	AI	RF input for lowband Rx (GSM900/GSM850)	VRF
TXO_HB	AO	RF output for highband Tx (DCS/PCS)	VRF
TXO_LB	AO	RF output pin for lowband Tx (GSM900/GSM850)	VRF
FREF1	AO	DCXO reference clock output	VRF
XTAL1	AIO	Input 1 for DCXO crystal	VRF
XTAL2	AIO	Input 2 for DCXO crystal	VRF
TP1	DI	GPI82	VRF
TP2	DI	GPI81	VRF
TP3	DI	GPI80	VRF
TP4	DO	GPO79	VRF

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Pin name	Type	Description	Power domain
CLK_SEL	AIO	DCXO mode selection	VRF
USB			
USB11_DM	AIO	D- data input/output	-
USB11_DP	AIO	D+ data input/output	-
Analog baseband			
HPR	AIO	Audio head phone output (R channel)	AVDD28_ABB
HPL	AIO	Audio head phone output (L channel)	AVDD28_ABB
HSP	AIO	Voice handset output (positive)	AVDD28_ABB
HSN	AIO	Voice handset output (negative)	AVDD28_ABB
AU_VIN0_P	AIO	Microphone 0 input (positive)	AVDD28_ABB
AU_VIN0_N	AIO	Microphone 0 input (negative)	AVDD28_ABB
AU_VIN1_P	AIO	Microphone 1 input (positive)	AVDD28_ABB
AU_VIN1_N	AIO	Microphone 1 input (negative)	AVDD28_ABB
AUX_IN4	AIO	Auxiliary ADC input	AVDD28_ABB
SPK_OUTP	AIO	Speaker positive output	VBAT_SPK
SPK_OUTN	AIO	Speaker negative output	VBAT_SPK
APC	AIO	Automatic power control DAC output	AVDD28_ABB
XP	AI	Touch anel X-axis positive input	AVDD28_ABB
XM	AI	Tou h panel X-axis negative input	AVDD28_ABB
YP	AI	Touch panel Y axis positive input	AVDD28_ABB
YM	AI	Touch panel Y-axis negative input	AVDD28_ABB
AU_MICBIAS0	AIO	Microphone bias source 0	AVDD28_ABB
AU_MICBIAS1	AIO	Microphone b as source 1	AVDD28_ABB
ACCDET	AIO	Accessory detec ion	AVDD28_ABB
Real-time clock			
XIN	AIO	Input pin for 32K cryst l	VRTC
XOUT	AIO	Input pin for 32K crystal	VRTC
XTAL_SEL	DIO	Pin option for external 32K crystal	VRTC
Power management unit			
VA	AIO	LDO output for ABB - VA	VBAT_ANALOG
VCAMA	AIO	LDO output for sensor – VCAMA	VBAT_VA
VCAMD	AIO	LDO output for sensor - VCAMD	VBAT_VA
VIBR	AIO	LDO output for vibrator - VIBR	VBAT_DIGITAL
VIO18	AIO	LDO output for 1.8V power - VIO18	VBAT_DIGITAL
VIO28	AIO	LDO output for 2.8V power - VIO28	VBAT_DIGITAL
VMC	AIO	LDO output for memory card - VMC	VBAT_DIGITAL
VSF	AIO	LDO output - VSF	VBAT_DIGITAL
VRF	AIO	LDO output for GSMRF - VRF	VBAT_VA
VRTC	AIO	LDO output for RTC - VRTC	VBAT_DIGITAL

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Pin name	Type	Description	Power domain
VSIM1	AIO	LDO output for 1st SIM - VSIM	VBAT_DIGITAL
VSIM2	AIO	LDO output for 2nd SIM - VSIM2	VBAT_DIGITAL
VUSB	AIO	LDO output for USB - VUSB	VBAT_DIGITAL
VCORE	AIO	LDO output for core circuit - Vcore	VBAT_DIGITAL
VREF	AIO	Band gap reference	BATSNS
VCDT	AIO	Charger-In level sense pin	BATSNS
DRV	AIO	IDAC current output open-drain pin	BATSNS
BATON	AIO	Battery Pack, NTC connected pin	BATSNS
ISENSE	AIO	Top node of current sensing 0.2ohm Rsense resistor	BATSNS
CHR_LDO	AIO	2.8V shunt-regulator output	BATSNS
BATDET	AIO	Battery detection pin	BATSNS
ISINK0	AIO	Backlight driver channel 0	VBAT_VA
ISINK1	AIO	Backlight driver channel 1	VBAT_VA
ISINK2	AIO	Backlight driver channel 2	VBAT_VA
ISINK3	AIO	Backlight driver channel 3	VBAT_VA
KPLED	AIO	Keypad led driver	VBAT_VA
FLYN	AIO	Charge pump flying cap negative terminal	AVDD43_CP
FLYP	AIO	Charge pump flying cap positive termin l	AVDD43_CP
TESTMODE	AIO	Test mode	BATSNS
PWRKEY	AIO	PWR key	BATSNS
Analog power			
AVDD28_FM	P	FM power	-
AVDD28_VRF	P	2.8V power supply for 2G RF	-
AVDD28_TCXO	P	2.8V power supply for 2G TCXO	-
AVDD28_2GAFE	P	2.8V power supply for 2G AFE	-
AVDD28_DBT	P	2.8V power supply for DBT	-
AVDD28_ABT	P	2.8V power supply for ABT	-
AVDD43_CP	P	VBAT input for charge pump	
VBAT_DIGITAL	P	Digital LDOs used battery voltage input	-
VBAT_VA	P	Analog LDOs used battery voltage input	-
VBAT_SPK	P	VBAT input for loud speaker driver	-
BATSNS	P	Battery node of battery pack	-
Analog ground			
AVSS28_ABB	G	ABB 2.8V ground	-
AVSS_BT	G	BT ground	-
AVSS_2G	G	2G RF ground	-
AVSS_FM	G	FM ground	-

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Pin name	Type	Description	Power domain
AVSS43_PMU	G	PMU ground	-
AVSS43_SPK	G	SPK ground	-
AGND	G	GND for VREF	-
AVSS43_CP	G	Charge pump GND	
Digital power			
DVDD28	P	2.8V power supply for digital macros in transceiver	-
DVDD28_FSRC	P	E-FUSE blowing power control	-
DVDD33_MSDC	P	3.3V memory card power	-
DVDD18_EMI	P	1.8V EMI IO power	-
DVDD28_SF	P	2.8V IO power	-
VDDK	P	1.2V core power	
Digital ground			
GND	G	Ground	-

Table 4. Acronym for state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 5. State of pins **Name**	**Reset**			**Output drivability**	**T rmination when not used**	**IO type**
	State[1]	**Aux**[2]	**PU/PD**[3]			
System						
RESETB	O	1	-	DIOH6/DIOL6	No need	IO Type 6
SRCLKENAI	I	7	PD	DIOH6/DIOL6	No need	IO Type 6
GPIO16	I	1	PD	DIOH2/DIOL2	No need	IO Type 1

[1] The column "State" of "Reset" shows the pin state during reset. (Input, High Output, Low Output, etc)

[2] The column "Aux" for "Reset" means the default aux function number, shown in the table "Pin Multiplexing, Capability and Settings".

[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

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Table 5. State of pins Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
GPIO17	I	1	PD	DIOH2/DIOL2	No need	IO Type 1
GPIO19	I	1	PD	DIOH2/DIOL2	No need	IO Type 1
EDI interfac						
EDICK	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EDIDAT	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EDIWS	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
RF control cir uitry						
BPI_BUS0	O	1	-	DIOH1/DIOL1	No need	IO Type 1
BPI_BUS1	I	1	PD	DIOH1/DIOL1	No need	IO Type 1
BPI_BUS2	O	1	-	DIOH1/DIOL1	No need	IO Type 1
BPI_BUS3	I	1	PD	DIOH1/DIOL1	No need	IO Type 1
UART interface						
URXD1	I	1	PU	DIOH3/DIOL3	No need	IO Type 3
UTXD1	O	1	-	DIOH1/DIOL1	No need	IO Type 1
URXD2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
UTXD2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
Keypad Interface						
KCOL0	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL1	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KCOL2	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KCOL3	I	0	PD	DIOH4/DIOL4	No need	IO Type 4
KCOL4	I	0	PD	DIOH4/DIO 4	No need	IO Type 4
KROW0	O	0	-	DIOH5/DIOL5	No need	IO Type 5
KROW1	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW2	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW3	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW4	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
Camera interface						
CMRST	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMPDN	O	0	-	DIOH1/DIOL1	No need	IO Type 1
CMVREF	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GMHREF	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT0	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT1	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT3	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT4	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT5	I	0	PD	DIOH1/DIOL1	No need	IO Type 1

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Table 5. State of pins **Name**	**Reset**			**Output drivability**	**Termination when not used**	**IO type**
	State[1]	**Aux[2]**	**PU/PD[3]**			
CMDAT6	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMDAT7	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMPCLK	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
CMMCLK	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
MS/SD card inte face						
MCINS	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
MCDA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA2	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA3	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCCM	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCMM0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
I2C interface						
SCL28	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
SDA28	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
LCD interface						
LSRSTB	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LSCE1B	O	1	-	DIOH2/DIOL2	No need	IO Type 2
LPCE0B	O	1	-	DIOH2/DIOL2	No need	IO Type 7
LPCE1B	O	1	-	DIOH2/DIOL2	No need	IO Type 2
LPTE	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LPRSTB	I	0	PD	DIOH2/DIO 2	No need	IO Type 2
LRD_B	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
LPA0	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
LWR_B	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
NLD8	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD7	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD6	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD5	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD4	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD3	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD2	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
NLD1	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
NLD0	I	0	PD	DIOH2/DIOL2	No need	IO Type 7
Watchdog reset						
WATCHDOG	O	1	-	DIOH1/DIOL1	No need	IO Type 1
General purpose I/O interface						
SFCS0	O	1	-	DIOH7/DIOL7	No need	IO Type 7

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Table 5. State of pins **Name**	**Reset**			**Output drivability**	**Termination when not used**	**IO type**
	State[1]	**Aux**[2]	**PU/PD**[3]			
SFCS1	I	0	PD	DIOH7/DIOL7	No need	IO Type 7
SIN	I	1	PU	DIOH7/DIOL7	No need	IO Type 7
SOUT	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SHOLD	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SWP	O	1	-	DIOH7/DIOL7	No need	IO Type 7
SCK	O	1	-	DIOH7/DIOL7	No need	IO Type 7

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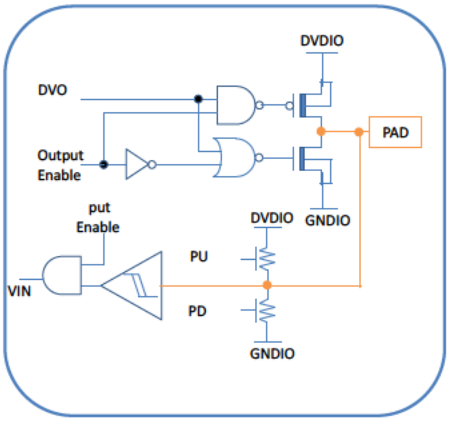
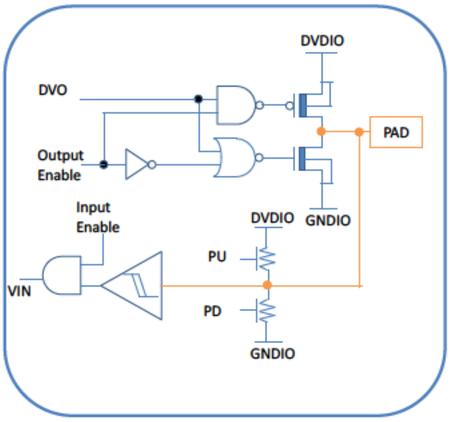
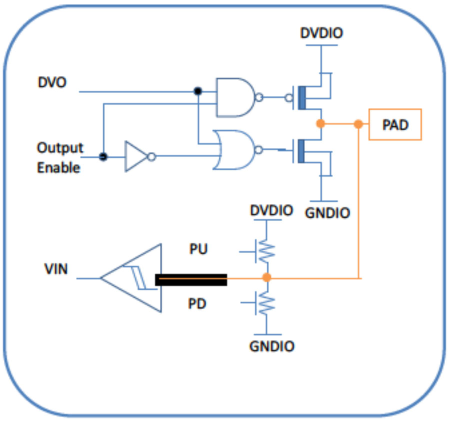


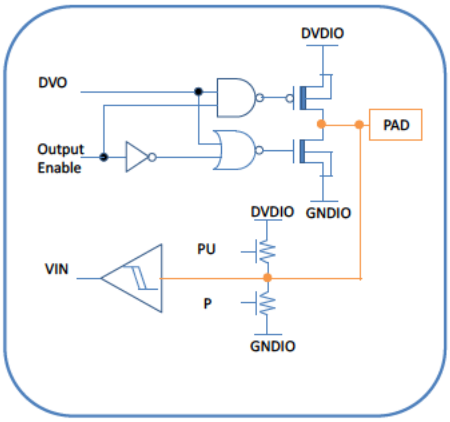
IO ty p1



IO tyep2



IO tyep3



IO tyep4

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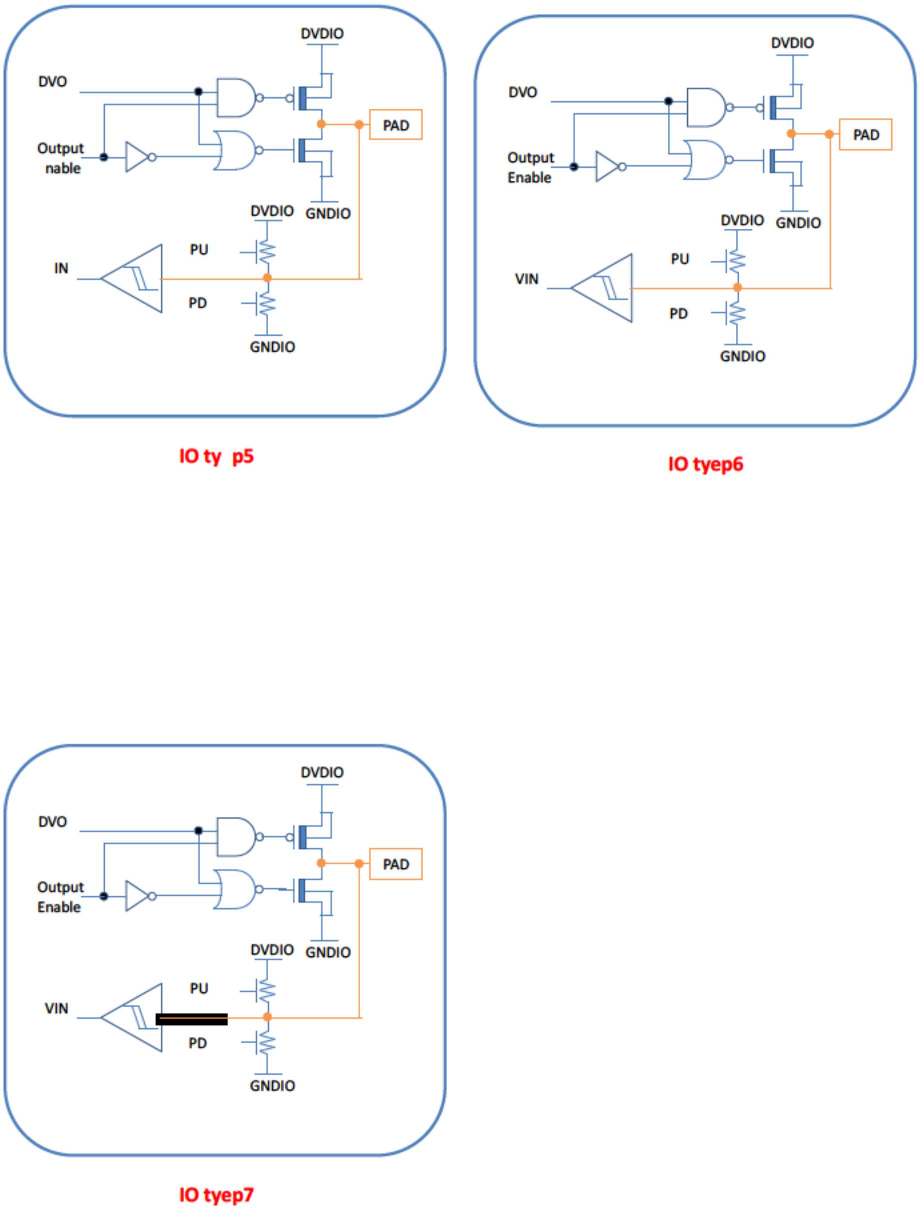

Figure 4. ***IO types in state of pins***

2.1.4 Pin Multiplexing, Capability and Settings

Table 6. ***Acronym for pull-up and pull-down types***

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Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 7. Capability of PU/PD, driving and Schmitt trigger

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
EDICK	0	GPIO0	IO	CU, CD	4, 8, 12, 16mA	0
	1	EDICK	O	-	4, 8, 12, 16mA	0
	2	PWM	O	-	4, 8, 12, 16mA	0
	3	EINT0	I	-	4, 8, 12, 16mA	0
EDIDAT	0	GPIO61	IO	CU, CD	4, 8, 12, 16mA	0
	1	EDIDAT	IO	CU, CD	4, 8, 12, 16mA	0
	2	PWM	O	-	4, 8, 12, 16mA	0
	3	EINT8	I	-	4, 8, 12, 16mA	0
EDIWS	0	GPIO18	IO	CU CD	4, 8, 12, 16mA	0
	1	EDIWS	O	-	4, 8, 12, 16mA	0
GPIO16	0	GPIO16	IO	CU CD	4, 8, 12, 16mA	0
	1	GPSFSYNC	O	-	4 8, 12, 16mA	0
GPIO17	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS5	O	-	4, 8, 12, 16mA	0
GPIO19	0	GPIO19	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS4	O	-	4, 8, 12, 16mA	0
SCL28	0	GPIO1	IO	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	SCL	IO	CU, CD	4, 8, 12, 16mA	0
	4	SPISCK0	O	-	4, 8, 12, 16mA	0
	5	D1_ICK	I	PD	4, 8, 12, 16mA	0
SDA28	0	GPIO2	IO	CU, CD	4, 8, 12, 16mA	0
	1	SDA	IO	CU, CD	4, 8, 12, 16mA	0
	4	SPICS0	O	-	4, 8, 12, 16mA	0
	5	D1_IMS	I	CU, CD	4, 8, 12, 16mA	0
KCLO4	0	GPIO5	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL4	IO	CU, CD	4, 8, 12, 16mA	0
	3	EIN 1	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTD	I	CU, CD	4, 8, 12, 16mA	0
	5	JDI		CU, CD	4, 8, 12, 16mA	0
	6	BTJDI	I	CU, CD	4, 8, 12, 16mA	0
KCOL3	0	GPIO6	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL3	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2CK	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	CU CD	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU CD	4 8, 12, 16mA	0
KCOL2	0	GPIO7	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL2	IO	CU, CD	4, 8 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	CU, CD	4 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8 12, 16mA	0
KCOL1	0	GPIO8	IO	CU, CD	4, 8, 12 16mA	0
	1	KCOL1	IO	CU, CD	4, 8, 12, 16mA	0
KCOL0	0	GPIO9	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCLO0	IO	CU, CD	4, 8, 12, 16mA	0
KROW4	0	GPIO11	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW4	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2WS	O	-	4, 8, 12, 16mA	0
	3	EINT3	I	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
KROW3	0	GPIO12	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW3	IO	CU, CD	4, 8, 12, 16mA	0
	2	EDI2DAT	O	-	4, 8, 12, 16mA	0
	4	FMJTDO	O	-	4, 8, 12, 16mA	0
	5	JTDO	O	-	4, 8, 12, 16mA	0
	6	BTJTDO	O	-	4, 8, 12, 16mA	0
KROW2	0	GPIO13	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW2	IO	CU, CD	4, 8, 12, 16mA	0
	5	JTRCK	O	-	4, 8, 12, 16mA	0
	6	BTDBGACKN	O	-	4, 8, 12, 16mA	0
KROW1	0	GPIO14	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW1	IO	CU, CD	4, 8, 12, 16mA	0
	5	DI_IDA	IO	PU, CD	4, 8, 12, 16mA	0
	6	BTDBGIN	I	CU, CD	4, 8, 12, 16mA	0
KROW0	0	GPIO15	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW0	IO	CU CD	4, 8, 12, 16mA	0
	2	LSDI0	I	CU, CD	4, 8, 12, 16mA	0
	4	CLKO6	O	-	4, 8, 12, 16mA	0
	5	LSCK0	O	-	4, 8, 12, 16mA	0
URXD2	0	GPIO20	IO	CU, CD	4, 8 12, 16mA	0
	1	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	2	U1RTS	O	-	4 8, 12 16mA	0
	3	BTPRI	IO	CU, CD	4, 8 12, 16mA	0
	4	SPIMISI0	O	-	4, 8, 12 16mA	0
UTXD2	0	GPIO21	IO	CU, CD	4, 8, 12, 16mA	0
	1	U2TXD	O	-	4, 8, 12, 16mA	0
	2	U1CTS	I	PU	4, 8, 12, 16mA	0
	3	CLKO0	O	-	4, 8, 12, 16mA	0
	4	SPIMISO0	I	PD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
URXD1	0	GPIO22	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1RXD	I	PU	4, 8, 12, 16mA	0
	4	EINT4	I	CU, CD	4, 8, 12, 16mA	0
UTXD1	0	GPIO23	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1TXD	O	-	4, 8, 12, 16mA	0
MCINS	0	GPIO24	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	EINT5	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
MCCK	0	GPIO25	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCK	IO	CU, CD	4, 8, 12, 16mA	0
	5	JRTCK	O	-	4, 8, 12, 16mA	0
MCDA0	0	GPIO26	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B		CU, CD	4, 8, 12, 16mA	0
MCDA1	0	GPIO3	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA1	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU CD	4, 8, 12, 16mA	0
	5	JTDI	I	CU, CD	4, 8, 12, 16mA	0
MCDA2	0	GPIO4	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA2	IO	CU, CD	4, 8, 12, 16mA	0
	2	WIFITOBT	I	CU, CD	4, 8 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	CU, CD	4 8, 12, 16mA	0
MCDA3	0	GPIO10	IO	CU, CD	4, 8 12, 16mA	0
	1	MCDA3	IO	CU, CD	4, 8, 12, 16mA	0
	3	EINT2	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	CU, CD	4, 8, 12, 16mA	0
MCCM0	0	GPIO27	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCM0	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDO	O	-	4, 8, 12, 16mA	0
	5	JTDO	O	-	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
NLD8	0	GPIO28	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD8	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMMCLK	O	-	2,4,6,8,10,12 ,14,16mA	0
NLD7	0	GPIO29	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD7	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSK	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
NLD6	0	GPIO30	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD6	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMRST	O	-	2,4,6,8,10,12 ,14,16mA	0
NLD5	0	GPIO31	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD5	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CM SD0	I	PD	2,4,6,8,10,12 ,14,16mA	0
NLD4	0	GPIO32	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD4	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMPDN	O	-	2,4,6,8,10,12 ,14,16mA	0
NLD3	0	GPIO33	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD3	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSDI3	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	5	CMCSD1	I	CU CD	2,4,6,8,10,12 ,14,16mA	0
NLD2	0	GPIO34	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD2	IO	PU CD	2,4,6,8,10,12 ,14,16mA	0
NLD1	0	GPIO35	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD1	IO	PU, CD	2,4,6,8,10,12 ,14,16mA	0
NLD0	0	GPIO36	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	NLD0	IO	PU, CD	2 4,6,8 10,12 ,14,16mA	0
	2	LSA0DA0	O	-	2,4,6,8,10,12 ,14,16mA	0
LWR_B	0	GPIO37	IO	CU, CD	2,4,6,8,10,12 14,16mA	0
	1	LWRB	O	-	2,4,6,8,10,12 ,14 16mA	0
	2	LSCK0	O	-	2,4,6,8,10,12 ,14 6mA	0
LRD_B	0	GPIO38	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LRDB	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LSDA0	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPA0	0	GPIO39	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPA0	O	-	2,4,6,8,10,12 ,14,16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	2	LSDI0	I	PD	2,4,6,8,10,12 ,14,16mA	0
LPCE0_B	0	GPIO40	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPCE0B	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	2	LSCE0B1	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LSCE1_B	0	GPIO41	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LSCE1B	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LPCE2B	O	-	2,4,6,8,10,12 ,14,16mA	0
	3	SCL	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPCE1_B	0	GPIO42	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPCE1B	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LPTE1	I	CU,CD	2,4,6,8,10,12 ,14,16mA	0
	3	SDA	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LSRSTB	0	GPIO43	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LSRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
WATCHDOG	0	GPIO44	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	WATCHDOG	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LPCE2B	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	EINT6	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
LPTE	0	GPIO45	IO	CU CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPTE1	I	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	3	CLKO1	O	-	2,4,6,8,10,12 ,14,16mA	0
LPRSTB	0	GPIO46	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	LPRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
	2	LSRSTB	O	-	2,4,6,8,10,12 ,14,16mA	0
	4	LPTE1	I	CU, CD	2 4,6,8 10,12 ,14,16mA	0
	5	LPCE3B	O	-	2,4,6,8,10,12 ,14,16mA	0
CMDAT0	0	GPIO47	IO	CU, CD	4, 8, 12 16mA	0
	1	CMDAT0	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	3	U2RTS	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
CMDAT1	0	GPIO48	IO	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	CMDAT1	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	3	U2CTS	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
CMDAT2	0	GPIO49	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT2	I	CU, CD	4, 8, 12, 16mA	0
	2	SCL	IO	CU, CD	4, 8, 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	CU, CD	4, 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8, 12, 16mA	0
CMDAT3	0	GPIO50	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT3	I	CU, CD	4, 8, 12, 16mA	0
	2	LRSTB	O	-	4, 8, 12, 16mA	0
	3	MC3CM0	IO	CU, CD	4, 8, 12, 16mA	0
	4	DAICLK	O	-	4, 8, 12, 16mA	0
	5	JTRCK	O		4, 8, 12, 16mA	0
	6	BTDBGACKN	O	-	4, 8, 12, 16mA	0
CMDAT4	0	GPIO51	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT4	I	CU CD	4, 8, 12, 16mA	0
	2	LSA0DA1	O	-	4, 8, 12, 16mA	0
	3	MC3DA0	IO	CU, CD	4, 8 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B	I	CU, CD	4 8, 12 16mA	0
	6	BTJTRST_B	I	CU, CD	4, 8 12, 16mA	0
CMDAT5	0	GPIO52	IO	CU, CD	4, 8, 12 16mA	0
	1	CMDAT5	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCK5	O	-	4, 8, 12, 16mA	0
	3	DAIPCMOUT	O	-	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	7	EGND48	I	PD	4, 8, 12, 16mA	0
CMDAT6	0	GPIO53	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT6	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDA1	IO	PU, CD	4, 8, 12, 16mA	0
	3	MC2DA2	O	-	4, 8, 12, 16mA	0
	4	DAIPCM N	I	-	4, 8, 12, 16mA	0
CMDAT7	0	GPIO54	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMDAT7	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDI1	I	CU, CD	4, 8, 12, 16mA	0
	3	MC3D 3	O	-	4, 8, 12, 16mA	0
	4	DAIPCMOUT	I	CU, CD	4, 8, 12, 16mA	0
CMHREF	0	GPIO55	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMHREF	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCE0B1	I	CU, CD	4, 8, 12, 16mA	0
	3	MC3CK	I	CU, CD	4, 8, 12, 16mA	0
	4	DAISYNC	O	-	4, 8, 12, 16mA	0
CMVREF	0	GPIO56	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMVREF	I	CU, CD	4, 8 12, 16mA	0
	2	SDA	IO	CU, CD	4, 8, 12, 16mA	0
	3	EINT7	I	PD	4, 8, 12, 16mA	0
	4	DAIRST	I	PD	4, 8, 12, 16mA	0
	5	LPTE0	I	PD	4, 8, 12 16mA	0
CMPDN	0	GPIO57	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPDN	O	-	4, 8, 12, 16mA	0
CMMCLK	0	GPIO58	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMMCLK	O	-	4, 8, 12, 16mA	0
CMPCLK	0	GPIO59	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPCLK	I	CU, CD	4, 8, 12, 16mA	0
	2	CMCSK	I	CU, CD	4, 8, 12, 16mA	0

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Name	**Aux. function**	**Aux. name**	**Aux. type**	**PU/PD/ CU/CD**	**Driving**	**SMT**
CMRST	0	GPIO60	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMRST	O	-	4, 8, 12, 16mA	0
EDIDAT	0	GPIO61	IO	CU, CD	4, 8, 12, 16mA	0
	1	EDIDAT	IO	CU,CD	4, 8, 12, 16mA	0
	2	PWM	O	-	4, 8, 12, 16mA	0
	3	EINT8	I	CU,CD	4, 8, 12, 16mA	0
BPI_BUS3	0	GPIO62	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS3	O	-	4, 8, 12, 16mA	0
BPI_BUS2	0	GPIO63	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS2	O	-	4, 8, 12, 16mA	0
BPI_BUS1	0	GPIO64	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS1	O	-	4, 8, 12, 16mA	0
BPI_BUS0	0	GPIO65	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPIBUS0	O	-	4, 8, 12, 16mA	0
SCK	0	GPIO69	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SCK	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SWP	0	GPIO67	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
	1	SWP	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SHOLD	0	GPIO72	IO	CU CD	2,4,6,8,10,12 ,14,16mA	0
	1	SHOLD	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SCS0	0	GPIO68	O	CU CD	2,4,6,8,10,12 ,14,16mA	0
	1	SCS0	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SCS1	0	GPIO66	O	CU, CD	2,4,6 8,10,12 ,14,16mA	0
	1	SCS1	O	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SIN	0	GPIO70	IO	CU, CD	2 4,6,8 10,12 ,14,16mA	0
	1	SIN	IO	CU, CD	2,4,6,8,10,12 ,14,16mA	0
SOUT	0	GPIO71	IO	CU, CD	2,4,6,8,10,12 14,16mA	0
	1	SOUT	IO	CU, CD	2,4,6,8,10,12 ,14 16mA	0
SRCLKENAI	0	GPIO73	IO	CU, CD	4, 8, 12, 16mA	0
	1	SRCLKENAI	I	CU, CD	4, 8, 12, 16mA	0
RESETB	0	GPIO74	IO	CU, CD	4, 8, 12, 16mA	0
	1	RESETB	IO	CU, CD	4, 8, 12, 16mA	0
XP	0	AGPIO75	IO	CU, CD	4, 8, 12, 16mA	0
	2	EINT30	I	CU, CD	4, 8, 12, 16mA	0

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Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
XM	0	AGPIO76	IO	CU, CD	4, 8, 12, 16mA	0
	2	EINT31	I	CU, CD	4, 8, 12, 16mA	0
YP	0	AGPIO77	IO	CU, CD	4, 8, 12, 16mA	0
	2	EINT32	I	CU, CD	4, 8, 12, 16mA	0
YM	0	AGPIO78	IO	CU, CD	4, 8, 12, 16mA	0
	2	EINT33	I	CU, CD	4, 8, 12, 16mA	0
TP4	0	AGPIO79	IO	CU, CD	4, 8, 12, 16mA	0
TP3	0	AGPIO80	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT34	I	CU, CD	4, 8, 12, 16mA	0
TP2	0	AGPIO81	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT35	I	CU, CD	4, 8, 12, 16mA	0
TP1	0	AGPIO82	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT36	I	CU, CD	4, 8, 12, 16mA	0

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 8. ***Absolute maximum r tings for power supply***

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	-0.3	+4.3	V
VBAT_ANALOG	Analog used battery voltage input	-0.3	+4.3	V
VBAT_SPK	VBAT input for loud speaker driver	-0.3	+4.3	V
VBAT_RF	RF used battery voltage input	-0.3	+4.3	V
VUSB	LDO output for USB-VUSB	+3.0	+3.6	V
AVDD28_FM	2.8V power supply for FM	+2.52	+3.08	V
AVDD28_2GAFE	2.8V power supply for 2G AFE	+2.52	+3.08	V
AVDD28_ABB	2.8V power supply for ABB	+2.52	+3.08	V
DVDD28	2.8V power supply for digital macros in transceiver	+2.52	+3 08	V
DVDD18	1.8V power supply for digital macros in transceiver	+1.62	+1.98	V
DVDD28_SF	2.8V IO power	+2.7	+3.6	V
	1.8V IO power	+1.7	+1.98	V
DVDD33_MSDC	3.3V memory card power	+3.0	+3.6	V

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Symbol or pin name	Description	Min.	Max.	Unit
DVDD18_EMI	1.8V EMI IO power	+1.62	+1.98	V
DVDD28_FSRC	E-FUSE blowing power control	+2.52	+3.08	V
VDDK	1.3v core power	+1.17	+1.43	V

Table 9. ***Absolute maximum ratings for voltage input***

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.08	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.08	V
VIN3	Digital input voltage for IO Type 3	-0.3	3.08	V
VIN4	Digital input voltage for IO Type 4	-0.3	3.08	V
VIN5	Digital input voltage for IO Type 5	-0.3	3.08	V
VIN6	Digital input voltage for IO Type 6	-0.3	3.08	V

Table 10. Absolu e maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	^{o}C

2.2.2 Recommended Operating Conditions

Table 11. ***Recommended operating c nditions for power supply***

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	3.4	3.8	4.2	V
VBAT_ANALOG	Analog used battery voltage input	3.4	3.8	4.2	V
VBAT_SPK	VBAT input for loud speaker driver	3 4	3.8	4.2	V
VBAT_RF	RF used battery voltage input	3.4	3.8	4.2	V
VUSB	LDO output for USB-VUSB	3.0	3.3	3.6	V
AVDD28_FM	2.8V power supply for FM	2.6	2 8	3.0	V
AVDD28_2GAFE	2.8V power supply for 2G AFE	2.65	2.8	2.95	V
AVDD28_ABB	2.8V power supply for ABB	2.6	2.8	3.0	V
DVDD28	2.8V power supply for digital macros in transceiver	2 7	2.8	2.9	V
DVDD18	1.8V power supply for digital macros in transceiver	1 62	1.8	1.98	V
DVDD28_SF	2.8V IO power	2 7	3.3	3.6	V
	1.8V IO power	1.7	1.8	1.98	

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD33_MSDC	3.3V memory card power	3.0	3.3	3.6	V
DVDD18_EMI	1.8V EMI IO power	1.62	1.8	1.98	V
DVDD28_FSRC	E-FUSE blowing powr control	2.7	2.8	3.08	V
VDDK	1.2v core power	1.17	1.3	1.43	VDDK

T ble 12. ***Recommended operating conditions for voltage input***

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V
VIN4	Digital input voltage for IO Type 4	-0.3	-	DVDIO+0.3	V
VIN5	Digital i put voltage for IO Type 5	-0.3	-	DVDIO+0.3	V
VIN6	Digit l input voltage for IO Type 6	-0.3	-	DVDIO+0.3	V
VIN7	Digital input voltage for IO Type 7	-0.3	-	DVDIO+0.3	V

Table 13. ***Recommended operating conditions for operating temperature***

Symbol or pin name	Description	Min.	Typ	Max.	Unit
Tc	Operating temperature	-20	-	85	^{o}C

2.2.18 Electrical Characteristics under Recommended Operating Conditions

Table 14. ***Electrical characteristics***

Symbol	Description	Condition	Min	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-5	-	5	µA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-5	-	5	
		PU enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-82.5	-	-6.1	μA
		PD enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-5	-	5	
		PU enabled, DVDIO = 1.8V, -0.3 VIN1 < 0.45	-35	-	0.8	μA
		PD enabled, DVDIO = 1 8V, -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH1	Digital high output current for IO Type 1	DVOH > 2.38V DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	12	-	-	mA
DIOL1	Digital low output current for IO Type 1	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH2	Digital high input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN2 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN2<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN2 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN2 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Dig tal I/O pull-down resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digit l output high voltage for IO Type 2	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL2	Digital o tput l w voltage for IO Type 2	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH3	Digital high input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-0 8	-	35	
DIIL3	Digital low input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-5	-	5	µA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-9.3	-	11.4	
DIOH3	Digital h gh output current for IO Type 3	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL3	Digital low output current for IO Type 3	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	DVD O = 2.8V	10	47	100	kΩ
		DVDIO = 1 8V	10	47	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL3	Digital output low voltage for IO Type 3	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH4	Digital high input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN4 < 2.1	-0.8	-	35	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIL4	Digi al low input current for IO ype 4	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-5	-	5	μA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-5	-	5	μA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN4 < 0.45	-9.3	-	11.4	
DIOH4	Digital high output current for IO Type 4	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL4	Digital low output current for IO Type 4	DVOL < 0 42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU4	Digital I/O pull-up resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD4	Digital I/O pull-down resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPU4 200K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	200	-	380	kΩ
DRPD4 200K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	200	-	380	kΩ
DVOH4	Digital output high voltage for IO Type 4	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL4	Digital output low voltage for IO Type 4	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH5	Digi al high input curren for IO Type 5	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN5 < 2.1	-0.8	-	35	
DIIL5	Digital low input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, -0.3 VIN5 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V -0.3 < VIN5 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN5 < 0.45	-9.3		11.4	
DIOH5	Digital high output current for IO Type 5	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL5	Digital low output current for IO Type 5	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DRPU5	Digital I/O pull-up resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD5	Digital I/O pull-down resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	40	75	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPU5 2K	Dig tal I/O pull-up resistance for IO Type 4 Key PAD mode)	DVDIO = 2.8V	1	-	2	kΩ
DRPD5 2K	Dig al I/O pull-down resistance for IO Type 4 (Key PAD m de)	DVDIO = 2.8V	1	-	2	kΩ
DVOH5	Digital output high voltage for IO Type 5	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL5	Digital output low voltage for IO Type 5	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH6	Digital high input current for IO Type 6	PU/PD disabled, D DIO = 2.8V, 2 1 < VIN6 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2 8V, 2.1 < VIN6 < 3.1	-22.5	-	12.5	
		PD enabled DVDIO = 2.8V, 2.1 < VIN6 < 3.1	6.1	-	82.5	
		PU/PD disable , DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-0.8	-	35	
DIIL6	Digital low input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-12.5	-	22.5	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-9.3	-	11.4	
DIOH6	Digital high output current for IO Type 6	DVOH > 2.38V, DVDIO = 2.8V	-8	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-6	-	-	mA
DIOL6	Digital low output current for IO Type	DVOL < 0.42V, DVDIO = 2.8V	-	-	8	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	6	mA
DRPU6	Digital I/O pull-up resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO 1.8V	70	150	320	kΩ
DRPD6	Digital I/O pull-down resistance for IO Type 6	DVD O = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH6	Digital output high voltage for IO Type 6	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL6	Digital output low voltage for IO Type 6	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH7	Digital high input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN7<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-11.4	-	9.3	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-0.8	-	35	
DIIL7	Digital low input current f r IO Type 7	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 VIN7 < 0.45	-9.3	-	11.4	
DIOH7	Digital high output current for IO Type 7	DVOH > 2.38V DVDIO = 2 8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL7	Digital low output current for IO Type 7	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU7	Digital I/O pull-up resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	50	320	kΩ
DRPD7	Digital I/O pull-down resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH7	Digital output high voltage for IO Type 7	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL7	Digital output low voltage for IO Type 7	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

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2.3 System Configuration

2.3.1 Strapping Resistors

Table 15. Strapping table

Pin name	Description	Trapping condition
CMPDN	Pull-up/down with 75K resister	Power-on reset
CMRST	Pull-up with 10K resister (Default internal Pull down with 75K resister)	Power-on reset/watchdog reset
BPI_BUS1	Pull up with 10K resister (Default internal Pull-down with 75K resister)	Power-on reset
BPI_BUS3	Pull-up with 10K resister (Default internal Pull-down with 75K resister)	Power-on reset

2.3.2 Mode Selection

Table 16. Mode selection of chip

Pin name	Description
XTAL_SEL	GND: Uses external 32K crystal as RTC clock source VRTC: Uses internal 32K as RTC clock source
CMPDN	GND: Uses 1.8V serial flash device DVDD28: Uses 3.3V erial ash device
KCOL0	GND: Boots ROM to enter USB download mode DVDD28: Normal boot-up mode
CMRST	GND: Disables USB download sub-feature to support virtual 2 USB com port DVDD28: Enables USB download sub feature to support virtual 2 USB com port
{BPI_BUS1,BPI_BUS3}	{GND, GND}: No JTAG {GND, DVDD28}: JTAG at keypad pins {DVDD28, GND}: JTAG at memory card pins {DVDD28, DVDD28}: JTAG at camera pins

2.3.3 Constant Tied Pins

Table 17. Constant tied pin of chip

Pin name	Description
TESTMODE	Tied to GND

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2.4 Power-on Sequence and Protection Logic

MT6260A provides 32K crystal removal feature. The XOSC32_ENB state tells if MT6260A provides this feature or not. VRF will be turned on at the same time with VRTC when XOSC32_ENB = 1. The power-on/off sequence controlled by "Control" and "Reset Generator" is shown as the figure below.

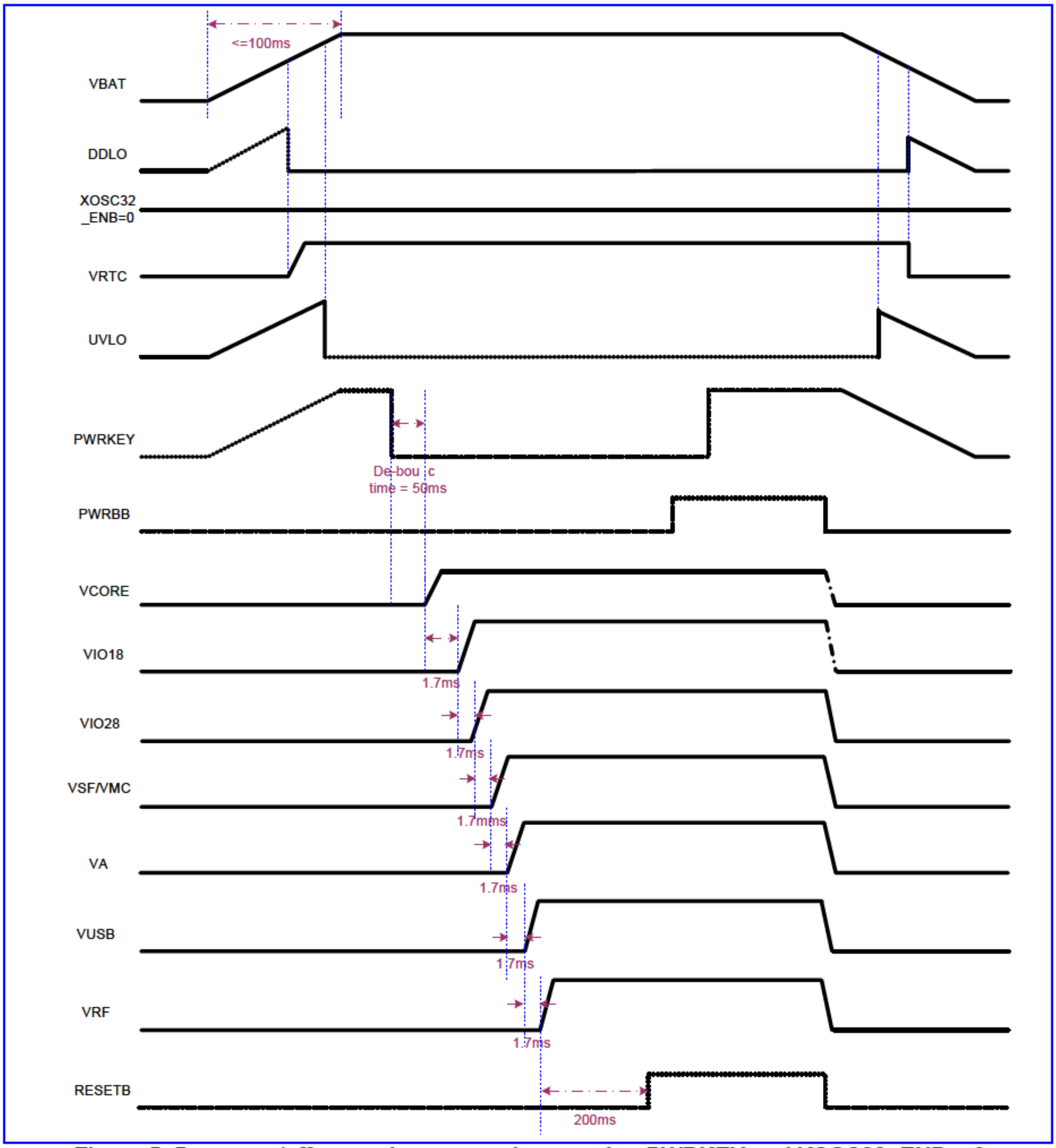

Figure 5. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 0

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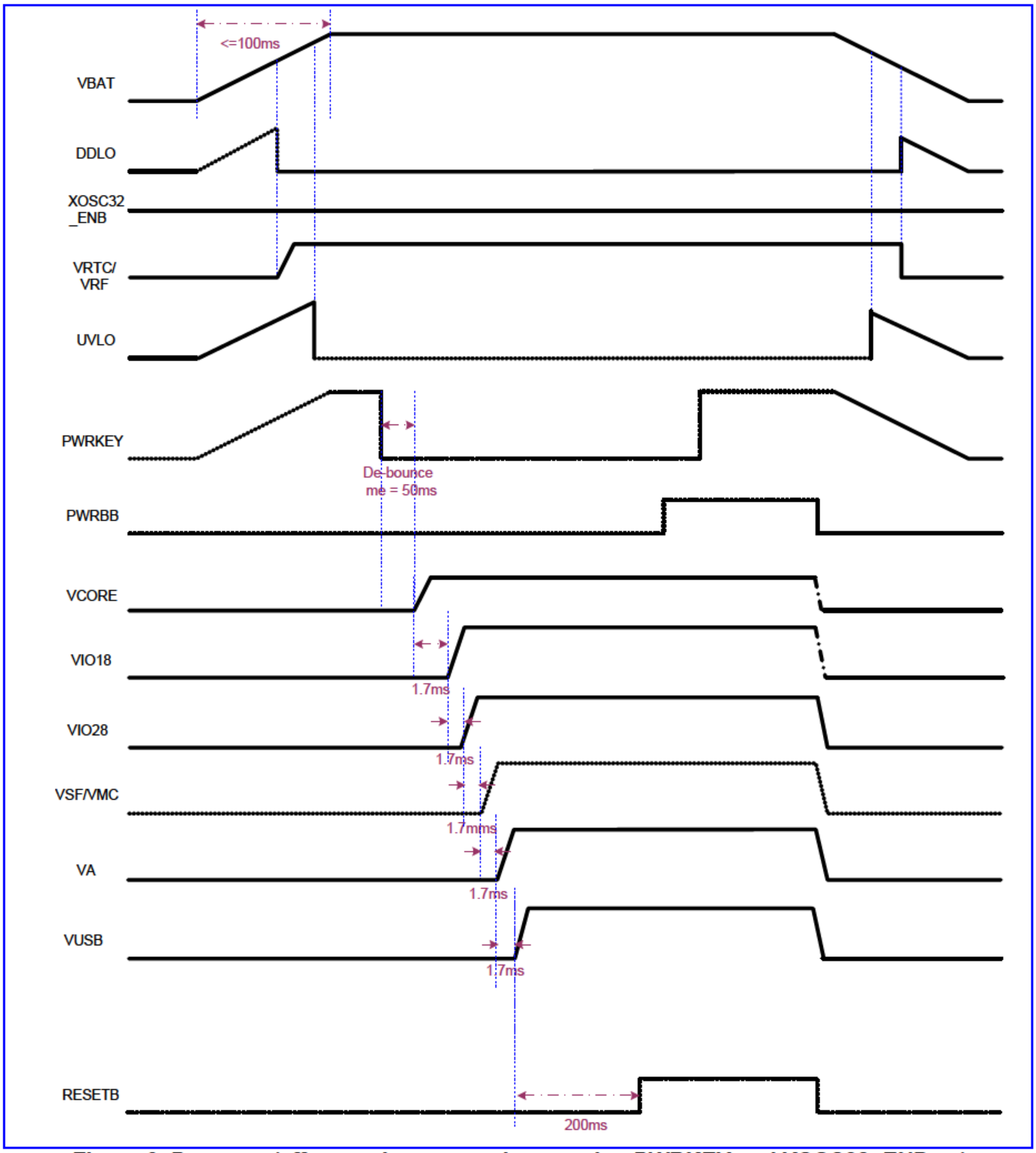

Figure 6. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 1

Note that each of the above figures only shows one power-on/off condition when XOSC32_ENB = 0 or XOSC32_ENB = 1. MT6260A handles the power-on and off of the handset. The following three methods can switch on the handset (when leaving UVLO): XOSC32_ENB = 0

1. Push PWRKEY (Pull the PWRKEY pin to the low level.)
   Pulling PWRKEY low is the typical way to turn on the handset. The turn-on sequence is VCORE → VIO18 → VIO28 → VSF, VMC → VA → VUSB → VRF

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The supplies for the baseband are ready, and the system reset ends at the moment when the above LDOs are fully turned on to ensure correct timing and function. After that, the baseband will send the PWRBB signal back to the PMU for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMU receives PWRBB from the baseband.

2. RTC modul generates PWRBB to wake up the system.
   If the RTC module is scheduled to wake up the handset at a certain time, the PWRBB signal will be directly sent to t e PMU. In this case, PWRBB will become high at specific moment and allow the PMU to be powered on as the sequence described above. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage is within the valid range.)
   The charger plug-in will also turn on the handset if the charger is valid (no OVP takes place). However, if the battery voltage is too low to power on the handset (UVLO state), the system will not be turned on by any of the three methods. In this case, the charger will charge the battery first and the handset will be powered on automatically as long as the battery voltage is high enough.

Under-voltage lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is p wered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures a smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself, except for VRTC LDO, to preven further discharging. Once the PMU enters the UVLO state, it will draw low quiescent current. The RTC LDO will still be working until the DDLO disables it.

Deep discharge lockout (DDLO)

The PMU will enter the deep discharge lockout (DDLO) s ate when the battery voltage drops below 2.5V. In this state, the VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or damage to the cells.

Reset

The PMU contains a reset control circuit which takes effect at both pow r-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter which uses the lock f om internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMU exceeds 150°C, the PMU will automatically disable all the LDOs except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the LDOs.

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2.5 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS baseband signal processing:

1. RF control: DAC for automatic power control (APC) is included, and its output is provided to external RF powe amplifier respectively.
2. Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring
3. Audio mixed-signal block: Provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and a plification for audio signals are also included.
4. Clock generation: Includes a clock squarer for shaping the system clock, and PLL providing clock signals to DSP, MCU and USB unit
5. XOSC32: A 32-kHz crystal oscillator circuit for RTC applications on analog blocks

2.5.1 APC-DAC

2.5.1.1 Block Description

APC-DAC is a 10-bit DAC with output buffer aiming at automatic power control. See the tables below for its analog pin assignment and functional specifi ation It is an event-driven scheme for power saving purpose.

2.5.1.2 Functional Specifications

Table 18. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Sampling rate			1.0833	MSPS
SINAD	Signal to noise and distortion ratio (10-kHz sine with 1.0V swing & 100-kHz BW)	47			dB
	99% settling time (full swing on maximal capacitance)			5	μS
	Output swing	0		AVDD	V
	Output capacitance		200	2200	pF
	Output resistance	0.47	10		KΩ
DNL	Differential nonlinearity for code 20 to 970		± 1		LSB
INL	Integral nonlinearity for code 20 to 970		± 1		LSB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 400 1		 μA μA

2.5.2 Auxiliary ADC

2.5.2.1 Block Description

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the seven auxiliary input pins. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 10-bit A/D converter: Conver the multiplexed input signal to 10-bit digital data.

Channel	Application	Input range [V]
0	BATSNS	3.2 ~ 4.2
1	ISENSE	3.2 ~ 4.2
2	VCDT	Decided by application circuit
3	BATON	0 ~ AVDD28
4	AUXIN4	0 ~ AVDD28
others	Internal use	N/A

2.5.2.2 Functional Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Table 19. Functional specifications of auxiliary ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FC	Clock rate		1.08		MHz
FS	Sampling rate @ N-Bit		1.08/(N+1)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel			 50 4	 fF pF
RIN	Input resistance Unselected channel Selected channel	 400 1			 MΩ MΩ

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Clock latency		N+1		1/FC
DNL	Differential nonlinearity		± 1		LSB
INL	Integral nonlinearity		± 1		LSB
OE	Offset error		± 10		mV
FSE	Full swing error		± 10		mV
SINAD	Signal to noise and distortion ratio (10-kHz full swing input & 1.0833-MHz clock rate)		50		dB
DVDD	Digit l power supply	1.1	1.2	1.3	V
AVDD	Analog powe supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 280 1		 μA μA

2.5.3 Audio Mixed-Signal Blocks

2.5.3.1 Block Description

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the figure below, it includes three parts. The first consists of stereo audio DACs and audio amplifiers for audio playback. The second part is the voice downlink path, including voice-band DACs (left channel audio DAC) and v ice amplifier, which produces voice signals to earphones or other auxiliary output devices. Amplifie s in the two blocks are equipped with multiplexers to accept signals from the internal audio/voice. Moreove , a ClassK amplifier is embedded to support continuous >1W output power with an on-chip charge-pump ev n under low battery scenario. The last part is the voice uplink path, which is the interface between the microphone (or other auxiliary input device) input and MT6260A DSP. A set of bias voltage is provided for the external electric microphone.

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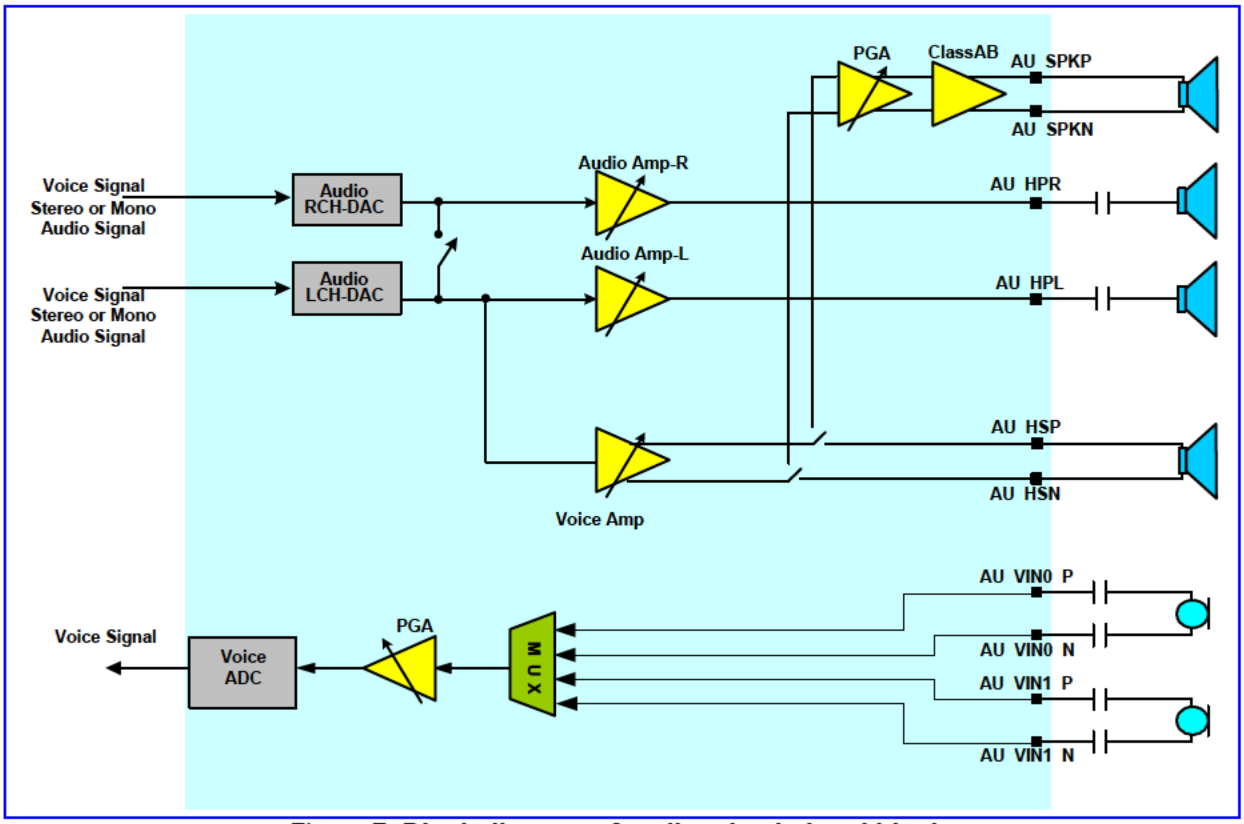

Figure 7. ***Block diagram of audio mixed-signal blocks***

2.5.3.2 Functional Specifications

See the table below for the functional specifications of voice band uplink/downlink blocks.

Table 20. Functional specifications of analog voice blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate		6,500		kHz
DVDD	Digital power supply	1.1	1 2	1.3	V
AVDD	Analog power supply	2.6	2 8	3.0	V
T	Operating temperature	-20		80	°C
VMIC	Microphone biasing voltage		1.9	2.2	V
IMIC	Current draw from microphone bias pins			2	mA
Uplink path[4]					
IDC	Current consumption for one channel		1.5		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dbm0	29			dB

[4] For uplink-path, not all gain settings of VUPG meet the specifications listed in the table, especially for several the lowest gains. The minimum gain that meets the specifications is to be determined.

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input level: 0 dbm0		69		dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBm0
Downlink path					
IDC	Current consumption		4		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	29	69		dB dB
RLOAD	Output resi tor load (differential)	16	32		Ω
CLOAD	Output capacitor load			250	pF
ICN	Idle channel noise of transmit path			-67	dBm0
XT	Crosstalk level on transmit path			-66	dBm0

See the table below for the func i nal specifications of audio blocks.

Table 21. Functional specifications of analog audio blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FCK	Clock frequency		6.5		MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2 6	2.8	3.0	V
T	Operating temperature	-20		80	°C
IDC	Current consumption		4		mA
PSNR	Peak signal to noise ratio		88		dB
DR	Dynamic range		88		dB
VOUT	Output swing for 0dBFS input level @ -1dB headphone gain		0.78		Vrms
$VOUT_{MAX}$	Maximum output swing		2.4		Vpp
THD	Total harmonic distortion 10mW at 64Ω load			-70	dB
RLOAD	Output resistor load (single-ended)	64			Ω
CLOAD	Output capacitor load			250	pF
XT	L-R channel cross talk	70			dB

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2.5.4 32-kHz Crystal Oscillator

2.5.4.1 Block Description

The low-power 32-kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors. See the figure below.

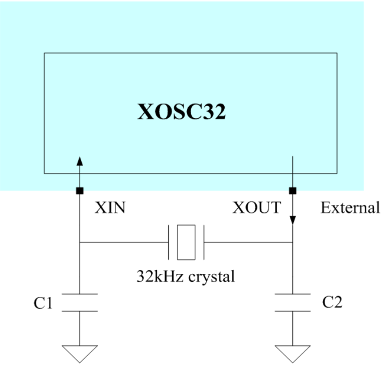

Figure 8. ***Block diagram of XOSC32***

2.5.4.2 Functional Specifications

See the table below for the functional specifications of XOSC32.

Table 22. Functional specifications of XOSC32

Symbol	Parameter	Mi	Typ.	Max.	Unit
AVDDR TC	Analog power supply	1	2.8		V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	30	50	70	%
	Current consumption			5	μA
T	Operating temperature	-25		70	°C

See the table below for recommendations on crystal parameters to use with XOSC32.

Table 23. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typ.	Max.	Unit
F	Frequency range		32,768		Hz
GL	Drive level			1	uW
Δf/f	Frequency tolerance		± 20		ppm
ESR	Series resistance		50	70	KΩ
C0	Static capacitance		0.9		pF

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Symbol	Parameter	Min.	Typ.	Max.	Unit
CL	Load capacitance		12.5		pF

2.6 Power Management Unit Blocks

The power management unit (PMU) manages the power supply of the entire chip, such as baseband, processor, memo y SIM cards, camera, vibrator, etc. The digital part of PMU is integrated into the analog part (see the igure below). PMU includes the following analog functions for signal processing:

- LDO: Regulates battery voltage to lower voltage level
- Charge pump BOOST (CP-BOOST): Boosts battery voltage to target voltage for Class-AB audio amplifier
- Keypad LED driver (KPLED) and current sink (ISINK) switches: Sink current for keypad LED and LCM module
- Start-up (STRUP): Generates power-on/off control sequence of start-up circuits
- Pulse charger (PCHR): Controls battery charging

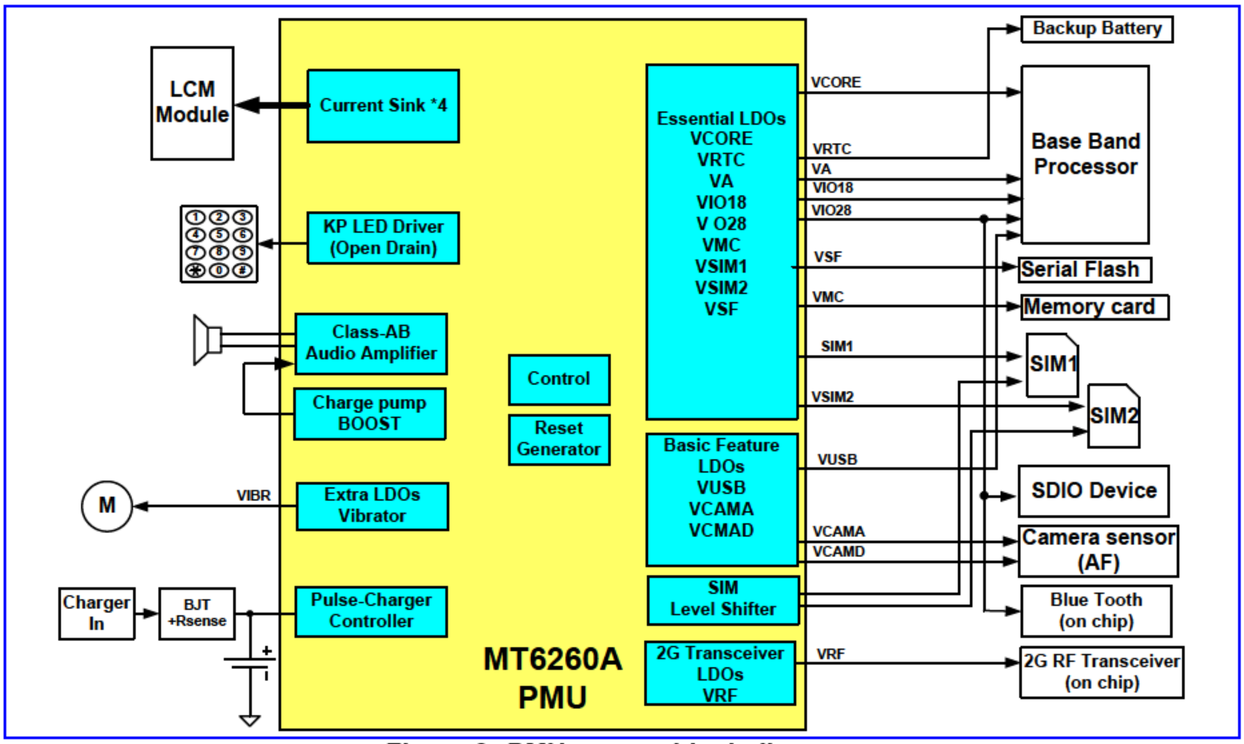

Figure 9. *PMU system block diagram.*

2.6.1 LDO

PMU integrates 14 general low dropout regulators (LDO) optimized for their given functions by balancing the quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

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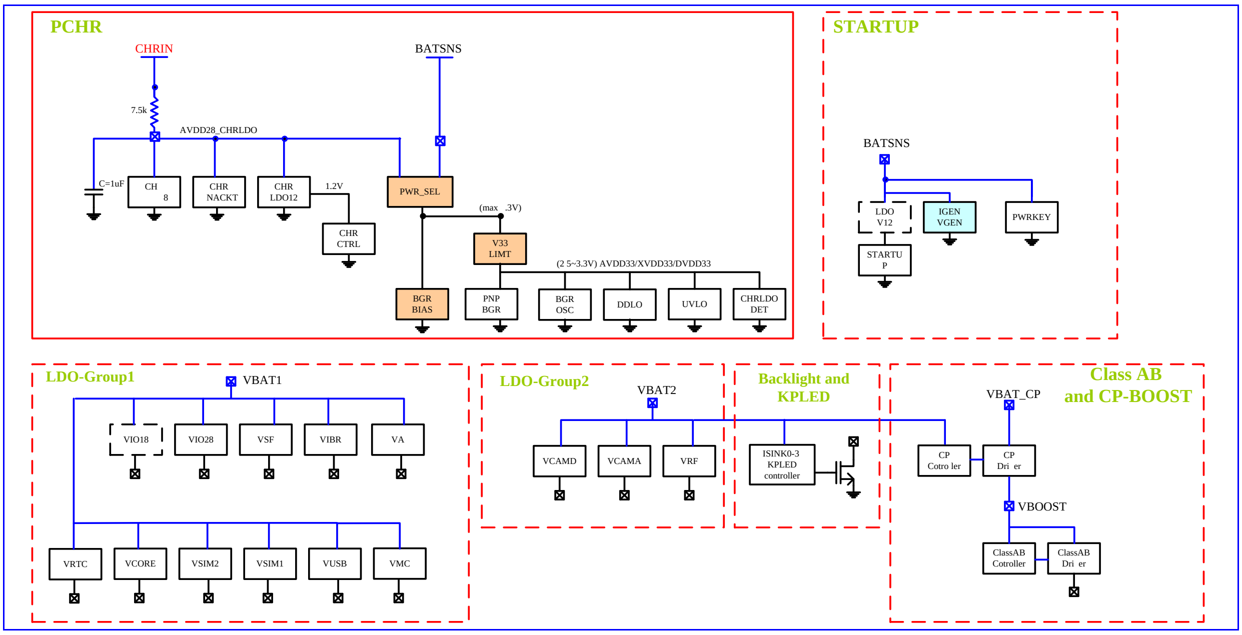

Figure 10. ***Power domain.***

2.6.1.1 LDO

The low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to   ery small differences between input and output voltages.

There are several features in the design of LDO, including discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be discharged first to avoid voltage accumulation on the capacitance. The soft-start limits inrush current and controls output-voltage rising time during power-up. The current limit is the current protection to limit the LDO's output current and power dissipation.

There are three types of LDOs in PMU of MT6260A. The analog LDO is optimized for low-frequency ripple rejection in order to reject the ripples coming from the burst of R   power amplifier. The digital IO LDO is a linear regulator optimized for very low quiescent current. The singl   step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features reverse current protection and is optimized for ultra low quiescent current while sustaining the RTC function as long as possible.

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2.6.1.1.1 Block Description

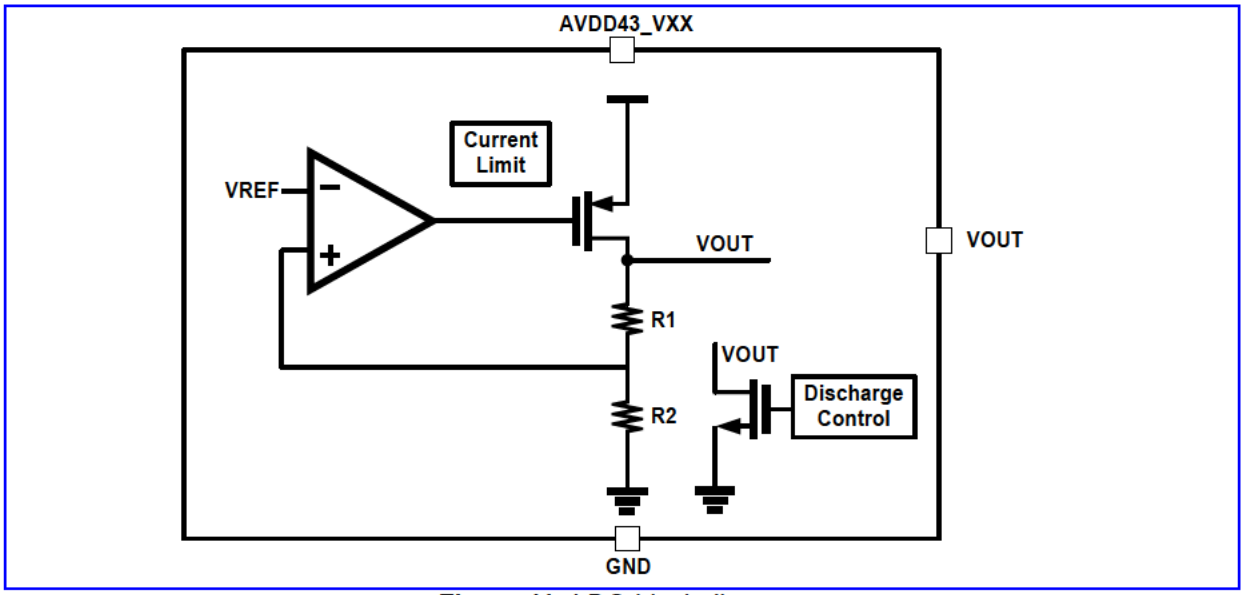

Figure 11. *LDO block diagram.*

2.6.1.1.2 LDO Types

Table 24. LDO types and brief specifications

Type	LDO name	Vout (Volt)	Imax(mA)	Description
ALDO	VRF	2.8	150	RF chip and 26MHz reference clock
ALDO	VA	2.8	150	Analog baseband
ALDO	VCAMA	2.8	150	Camera sensor
DLDO	VIO28	2.8	100	Digital IO and Blue tooth
DLDO	VSIM	1.8/3.0	30	SIM card
DLDO	VSIM2	1.8/3.0	30	SIM card
DLDO	VUSB	3.3	50	USB
DLDO	VIO18	1.8	100	Digital IO
DLDO	VCORE	0.75~1.3	250	Digital baseband
DLDO	VCAMD	1.8/2.8	100	Camera sensor
DLDO	VIBR	1.8/2.8/3.0	150	Vibrator, drop out <400mV at 150mA loading

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Type	LDO name	Vout (Volt)	Imax(mA)	Description
DLDO	VMC	2.8/3.0/3.3	200	Memory card, drop out <400mV at 200mA loading
DLDO	VSF	1.86/3.3	50	Serial flash
RTCLDO	VRTC	2.8	2	Real-time clock

2.6.1.1.3 Functional Specifications

Table 25. Analog LDO specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		μF
	Vout	Includes load regulation, line regulation, and tem erature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C
	PSRR	Iout < 0.5*Imax 10 < f < 3 kHz	65			dB
		Iout < 0.5*Imax 3K < f< 30 kHz	45			dB
	Output noise	With A-weighted filter			90	uVrms
	Quiescent current	Iout = 0		55		μA
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	μsec

Table 26. Digital LDO specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1[5]		μF
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%,		Max. (+5%,	V

[5] VCORE loading capacitor typical value is 2.2uF. Other LDOs are 1uF.

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
			-0.1V)		+0.1V)	
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout = 0		15		μA
	Turn on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn on settling time	Iout = 0			240	μs

Table 27. RTC LDO specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		μF
	Vout	Includes load regulation, line regulation, and temperature coefficient	2	2.8	3	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout 0		15		μA

2.6.2 Charge Pump BOOST

2.6.2.1 Functional Specifications

Table 28 . Charge pump BOOST specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Cfly Chold			4.7 4.7		μF
	Vout			4.2		V
	Ripple	Vin=3.4~4.05V Cfly/Cout=4.7uF/4.7uF @ Iload=250mA			200	mV
	Switching frequency			600		KHz
	Quiescent current	Iout = 0		4	6	mA

2.6.3 ISINK and KPLED Switches

One built-in open-drain output switch drives the keypad LED (KPLED) in the handset. The switch is controlled by the baseband with enabling registers. The switch of keypad LED can sink as much as 60mA current, and the output is high impedance when disabled. The value of the sink current decides the brightness of the LED.

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Four current controlled open drain drivers (ISINK0 ~ 3) are also implemented to drive the LCM backlight module, and each channel provides 6-current-level steps of up to 24mA. The maximum current-level can be extended to 48mA by doubling the current-level through register settings.

2.6.3.1 Block Description

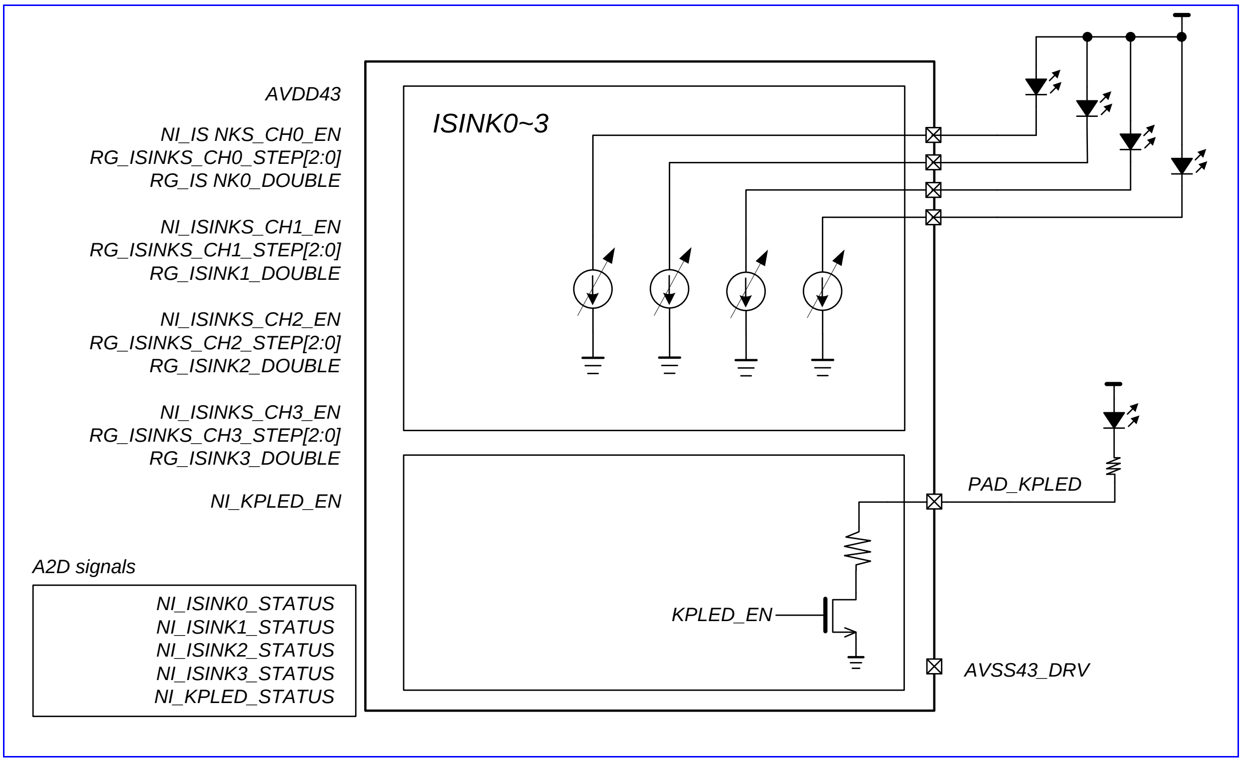

Figure 12. *ISINKs and KPLED switches bock diagram.*

2.6.3.2 Functional Specifications

Table 29. ISINKs and KPLED Switches Sp cification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Sink current of keypad LED driver	Von > 0.5V, 100% dimming duty	60			mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 000		4		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 001		8		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 010		12		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP =		16		mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		011				
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 100		20		mA
	Sink current of ISINK0 ~ 3	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 101		24		mA
	Current mismatch be ween the 4 channels	Von > 0.15V, 100% dimming duty	-5		5	%

2.6.4 STRUP

PMU handles the power-on and off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.4V) nor in the therma condition, there are three methods to power on the handset system: pulling PWRKEY low (the use pushes PWRKEY), pulling PWRBB high (baseband BB_WakeUp) or valid charger plug-in.

According to different battery voltage (VBAT) and phone states, control signals and regulators will have different responses.

2.6.5 PCHR

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a p e-determined range, the charging process will be activated. This detector can resist higher input oltage than other parts of the PMU(30V for max. rating voltage, 7V for max. operation range).

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2.6.5.1 Block Description

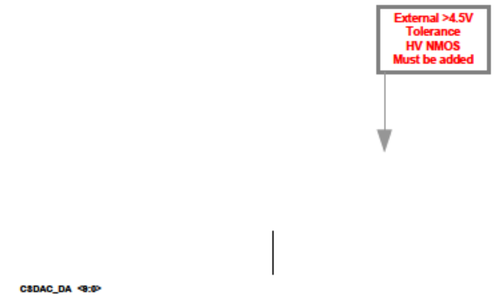

Figure 13. *PCHR block diagram.*

2.6.5.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0 V), the charger detector stops the charging process immediately to avoid burning out the chip or even the phone. In addition, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

2.6.5.1.2 Charging Control

When the charger is active, the charger controller manages the charging phase accord ng to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMU power-off state), CC mode (constant current mode or fast charging mode at the range 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. The charging states diagram is shown in the figure below.

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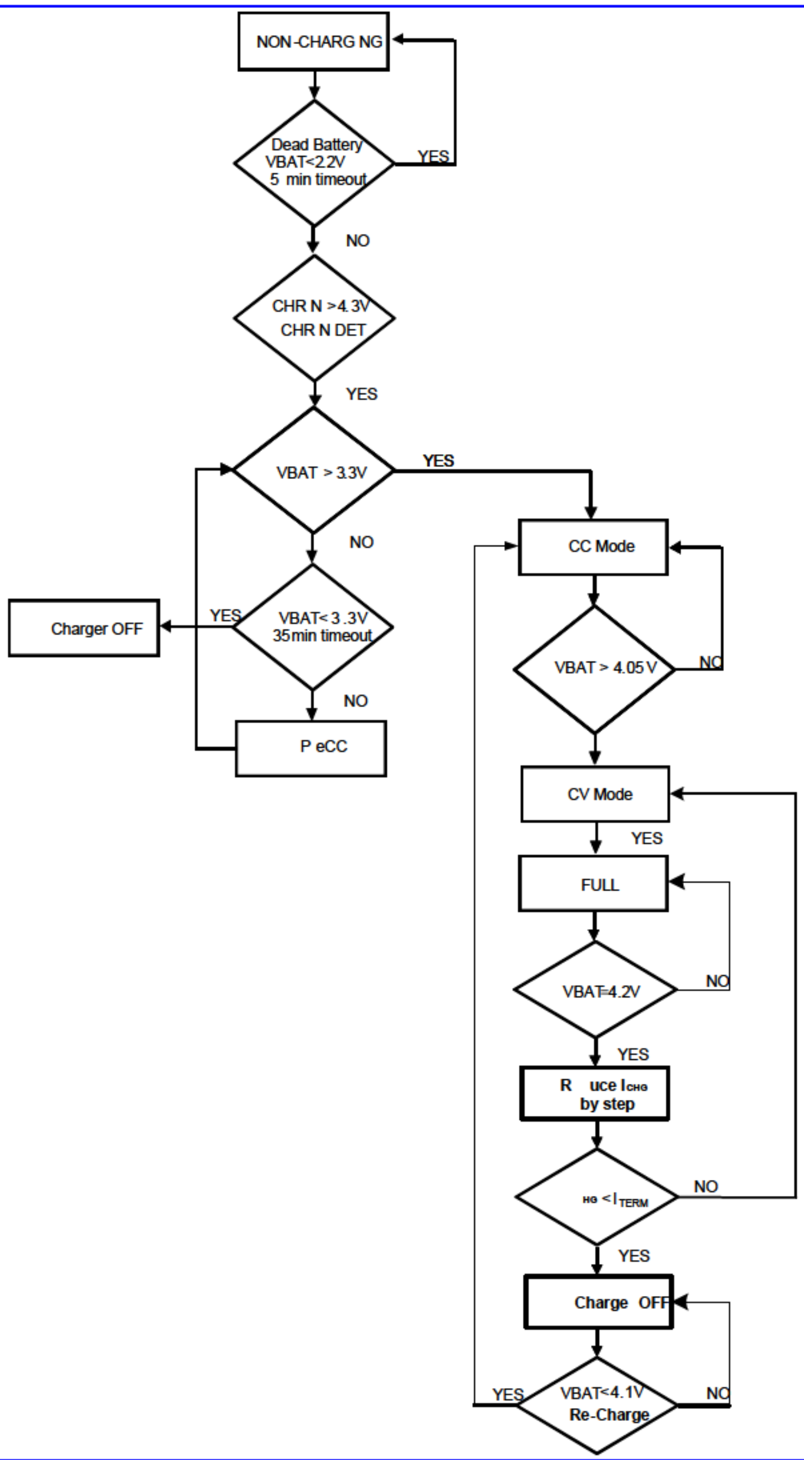

Figure 14. ***Charging states diagram***

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger operates in the pre-charge mode. There are two steps in this mode. When the battery voltage is deeply discharged below 2.2V, PRECC0 trickle charging current will be applied to the battery.

The PRECC1 trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery oltage exceeds 2.2V, called the PRECC2 stage, the closed-loop pre-charge is enabled. The voltage drop across the external RSENSE is kept around 40mV (AC charger) or 14mV (USB host). The clos d-loop pre-charge current can be calculated:

$$I_{PRECC2,AC\ adapter} = \frac{V_{SENSE}}{Rsense} = \frac{40mV}{Rsense}$$

$$I_{PRECC2,USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3 4V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents c n be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 800mA. It can a commodate the battery charger to various charger inputs with different current capabilities.

Constant voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a consta t v ltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in orrespondence to a linear charger. While the battery voltage actually reaches 4.2V, the charging cu rent is gradually decreased step-by-step, the end-of-charging process starts. It may prolong the ch ging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches zero automatically and this mechanism is optimized for different battery

BC1.1 Dead-Battery Support of China Standard

MT6260A supports dead-battery condition from China standard (called BC1.1). The specification protects dead-battery charging by timer and trickle current. Once the battery vo tage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying trickle current, the charger will be disabled. On the other hand, if the battery voltage is raised to above 2.2V, the charger will enter the PRECC2 stage, and the charging current will be 70mA or 200mA depending on the type of charging port.

Under the condition of battery voltage from 2.2V to 3.3V, the charger will charge the battery with the PRECC2 current.

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A dedicated 5mins (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35mins (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.3V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

2.6.5.2 Functional Specifications

Table 30. Charger detection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charger detect-on range		4.3		7	V

Table 31. Pre-charge specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	IUNIT with 500ms pulse	VBAT < 2.2V	28	56	84	mA
	Pre-charging current	VBAT .2V (500ms pulse)	28	56	84	mA
		VBAT ≥ 2.2V (USB host)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter < 7V)	$30/R_{sense}$	$40/R_{sense}$	$50/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter > 7V)	$7\ R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
	Pre-charging off threshold	CHR_EN = L		3.3		V
	Pre-charging off hysteresis			0.4		V

- *Table 32.* Constant current specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	CC mode charging current (CS_VTH)	CS_VTH [2:0] = 000		$160/R_{sen\ e}$		mA
		CS_VTH [2:0] = 001		$140/R_{sense}$		mA
		CS_VTH [2:0] = 010		$130/R_{sense}$		mA
		CS_VTH [2:0] = 011		$110/R_{sense}$		mA
		CS_VTH [2:0] = 100		$90/R_{sense}$		mA
		CS_VTH [2:0] = 101		$60/R_{sense}$		mA
		CS_VTH [2:0] = 110		$40/R_{sense}$		mA
		CS_VTH [2:0] = 111		$14/R_{sense}$		mA

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Current sensing resistor	RSENSE		0.2		ohm

Table 33. ***Constant voltage and over-voltage protection specifications***

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Ch rging complete threshold		4.15	4.2	4.25	V
	Battery over-voltage protection threshold (OV)			4.3		V

Table 34. BC1.1 specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
IUNIT	BC1.1 trickle curr nt	VBAT < 2.2V		56	100	mA
IPRECC1 (USB host)	PRECC1 current	2.2 < VBAT < 3.3V		70	100	mA
IPRECC1 (AC adapter)	PRECC1 current	2.2 < VBAT < 3.3V		200	250	mA
T1	5 minute dedicated timer	2.2 VBAT < 2.7V		5	7	min.
T2	35 minute dedicated timer	2.7 < VBAT < 3.3V		35	36	min.
TUNIT	BC1.1 trickle current period				1	sec.

USBDL without battery

The flash tool can download firmware from PC to cell phone without plugging in a valid battery (i.e. > UVLO, 3.2V) through this feature named "USBDL w/o battery". This feature provides the needed power from the adaptor to the system. MT6260A provides two methods for downloading without battery: Auto-Power-On (APO) and pressing download key (DLKEY). APO is activated automatically when no battery is inserted and an valid adaptor is plugged in. APO can source a typical current level of 450mA from the adaptor, and the current can be confined within a maximum level determined by a fixed and pre-defined setting and the external power device's current gain (i.e. β of th B T) You can also enable USBDL w/o battery by pressing DLKEY. This auxiliary DL function supports a system with a battery that has no NTC pin. For this specific scenario, the BATON pin of MT6260A is recommended to be tied to the ground. On top of that, pressing DLKEY is the only way to conduct USBDL. Moreover, the current level is the same as that of APO. The current lasts for 8 seconds and can be programmed once SW can control the system. During DL, VBAT is limited by a default OV level of 4.2V to avoid over-stressing on the internal components.

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2.7 GSM/GPRS/EDGE-Rx RF

2.7.1 General Description

2G RFSYS which is built in MT6260A SOC is a highly integrated RF transceiver for multi-band GSM, GPRS and EDGE-Rx cellular systems.

The features include:

Receiver

- Single-end saw-less Rx
- Quadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 12dB PGA gain with 6dB g in step

Transmitter

- High accurate transmitter modulat r for GSM/GPRS application
- Built-in calibration of SX loop filter and loop gain

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GSM/GPRS/EDGE-Rx applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin26 MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Supports 32K XTAL-less operation

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2.7.2 Functional Block Diagram

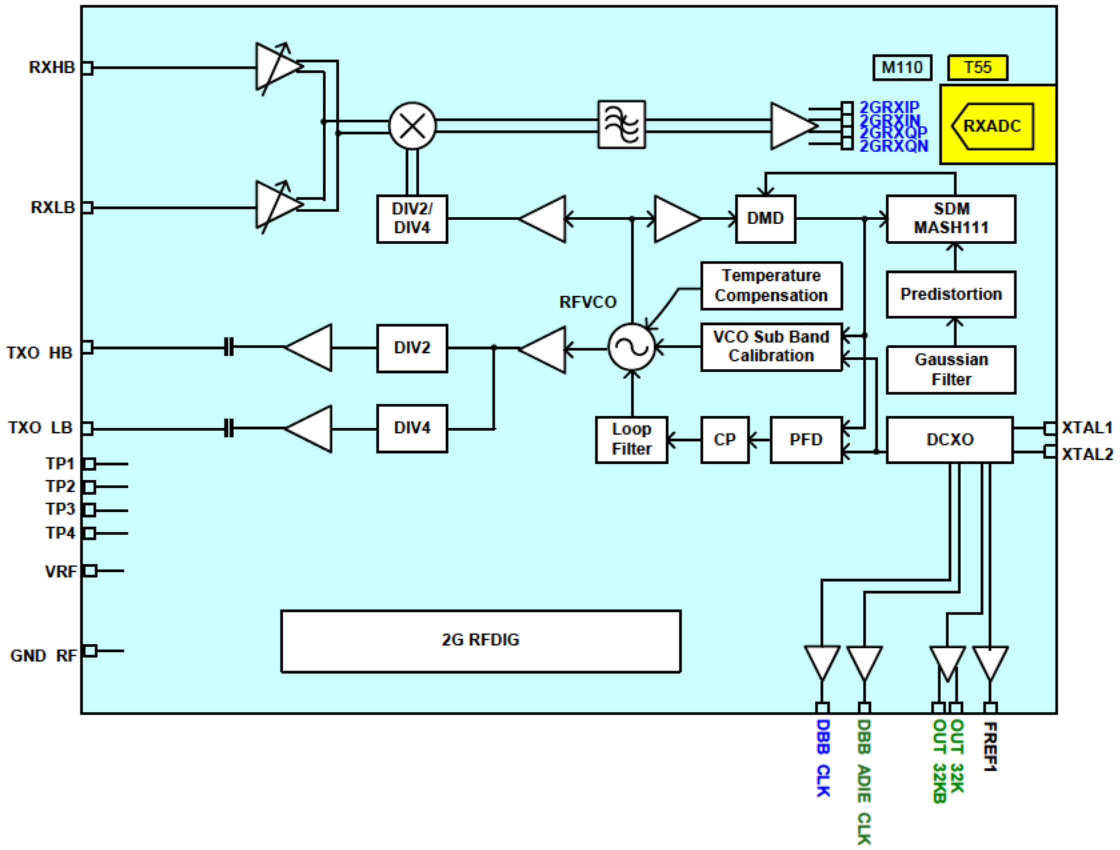

Figure 15. ***Diagram of MT6260A 2G RFSYS***

2.7.3 Electrical Characteristics

Table 35. DC characteristics (TA = 25oC, VDD = 2.8V un ess otherwise stated)

RFSYS mode	VRF	AVDD28_2GAFE	RFSYS total	Unit
BCM_Deep sleep (DCXO is off)	17	1	18	uA
BCM_Sleep (DCXO is on)	2.8	0.26	3.	mA
Low power mode	65	1	66	uA
Full power mode	2.8	0.26	3.1	mA
RX (GSM850/EGSM)	64	5	69	mA
RX (DCS/PCS)	74	5	79	mA
TX (GSM850/EGSM)	52	2	54	mA
TX (DCS/PCS)	47	2	49	mA

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Table 36. Rx AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Input frequency	F_{RX}	GSM850		869		894	MHz
		GSM900		925		960	MHz
		DCS1800		1,805		1,880	MHz
		PCS1900		1,930		1,990	MHz
Voltage gain 1	G_1	GSM850	LNA = High gain PGA = Middle high gain	52[1]	55		dB
		GSM900		52[2]	55		dB
		DCS1800	LNA = High gain PGA = Middle high gain	52[3]	55		dB
		PCS1900		52[4]	55		dB
Voltage gain 2	G_2	GSM850	LNA = Middle high gain PGA = Middle high gain		51		dB
		GSM900			51		dB
		DCS1 00	LNA = Middle high gain PGA = Middle high gain		53		dB
		PCS1900			53		dB
Voltage gain 3	G_3	GSM850	LNA = Middle gain PGA = Middle high gain		49		dB
		GSM900			49		dB
		DCS1800	LNA = Middle gain PGA = Middle high gain		50		dB
		PCS1900			50		dB
Voltage gain 4	G_4	GSM850	LNA = Low gain PGA = Middle high gain		26.5		dB
		GSM900			26.5		dB
		DCS1800	LNA = Low gain PGA = Middle high gain		28		dB
		PCS1900			28		dB
Noise figure at 25°C	NF_{25}	GSM850	G_1		4	6[1]	dB
		GSM900			4	6[2]	dB
		DCS1800			4	6[3]	dB
		PCS1900			4	6[4]	dB
Noise figure at 85°C	NF_{85}	GSM850	G_1		5		dB
		GSM900			5		dB
		DCS1800			5		dB
		PCS1900			5		dB
2nd-order input intercept point	IIP2	GSM850	G2	31[1]	43		dBm
		GSM900		31[2]	43		dBm
		DCS1800		31[3]	43		dBm

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Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
		PCS1900		31[4]	43		dBm
3rd-order input intercept point	IIP3	GSM850	G2	-14[1]	-3		dBm
		GSM900		-14[2]	-3		dBm
		DCS1800		-14[3]	-3		dBm
		PCS1900		-14[4]	-3		dBm
3rd-order input intercept point @ -20°C	$IIP3_{-20}$	GSM850	G2		-5		dBm
		GSM900			-5		dBm
		DCS1800			-5		dBm
		PCS1900			-5		dBm
Receiver S/N with 3MHz blocker	SN_{3M}	GSM850	G2 Blocker = -23dBm	8[1]	12		dB
		GSM900		8[2]	12		dB
		DCS1800	G2 Blocker = -26dBm	8[3]	12		dB
		PCS1900		8[4]	12		dB
Receiver S/N with OBB	SN_{OOB}	GSM 50	G3 Blocker = 2dBm, offset 20MHz	6[5]	8		dB
		GSM900		6[5]	8		dB
		DCS1800	G3 B ocker = 2dBm, offse 80MHz	6[5]	8		dB
		PCS1900		6[5]	8		dB
Image rejection ratio	IRR	ALL	G2	32[1,2,3,4]	40		dB
Receiver channel response attenuation		ALL	@3MHz offset		20		dB
			@6MHz offset		35		dB
Receiver filtering 3-dB bandwidth		ALL	For all gain settings		900		kHz
PGA gain linearity		ALL	INL		0.2	1[5]	dBΩ
			DNL		0 1	0.5[5]	dBΩ
PGA gain step		ALL			6		dBΩ
PGA dynamic range		ALL			12		dBΩ
I/Q common-mode output voltage		ALL	G1	1.1[5]	1.2	1.3[5]	V
Output static dc offset		ALL	G1		100	200	mV

Table 37. Tx GMSK AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

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Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Frequency	F_{TX}	GSM850		824		849	MHz
		GSM900		880		915	MHz
		DCS1800		1,710		1,785	MHz
		PCS1900		1,850		1,910	MHz
RMS phase e ror	PE_{rms}	GSM850 GSM900			1.5	2.5[1,2]	degree
		DCS1800 PCS1900			1.5	2.5[3,4]	degree
Output modulation spectrum	ORFS	GSM850 GSM900	400kHz offset (RBW = 30kHz bandwidth)		-66	-64[1,2]	dBc
		DCS1800 PCS1900			-66	-64[3,4]	dBc
		GSM850 GSM900	1.8MHz offset (RBW = 30kHz bandwidth)			-75[5]	dBc
		DCS1800 PCS1900				-75[5]	dBc
Tx noise in Rx band		GSM850	20MHz offset		-165	-164[5]	dBc/Hz
			35MHz offset		-168	-167[5]	dBc/Hz
		GSM900	20MHz offset		-165	-164[5]	dBc/Hz
			35MHz offset		-168	-167[5]	dBc/Hz
		DCS1800	20MHz offset		-160	-156[5]	dBc/Hz
		PCS1900	20MHz of set		-160	-156[5]	dBc/Hz
Output power level	P_{out}	GSM850 GSM900	PA driver amplifier R_{load} = 50Ω	1[1,2]	3	6[1,2]	dBm
		DCS1800 PCS1900		1[3,4]	3	6[3,4]	dBm
Output 3rd harmonics		ALL	PA driver amplifier		-10		dBc

Table 38. SX AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit
Frequency range	F_{range}		3,296		3,980	MHz
Reference frequency	F_{ref}			26		MHz
Frequency step resolution	F_{res}			3		Hz
Phase noise	PN_{10k}	@ 10kHz offset		-83		dBc/Hz
	PN_{400k}	@ 400kHz offset		-116		dBc/Hz
	PN_{3M}	@ 3MHz offset		-136		dBc/Hz

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Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Lock time of Rx burst	T_{lock_rx}	Frequency error < ± 0.1ppm		150	200[5]	us
Lock time of Tx burst	T_{lock_tx}	Frequency error < ± 0.1ppm		200	300[5]	us
Pushing figure		With internal RFVCO LDO		400		kHz/V

Table 39. DCXO AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating frequency	F_{ref}			26		MHz
Crystal C load	C_L			7.5		pF
Crystal tuning sensitivity	T_S		27.5	32.3		ppm/pF
Static range	SR	CDAC from 0 to 255	± 22	± 50		ppm
Dynamic range	DR	CAFC from 0 to 8191	36	50		ppm
AFC tuning step	$F_{res\text{-}AFC}$			0.006		ppm/DAC
AFC settling time	T_{AFC}	CAFC from 0 to 8191 CAFC from 8191 to 0 Frequency er or < 0.1ppm		100	200[5]	us
Start-up time	T_{DCXO}	Frequency e ror < 1ppm Amplitude > 90 %			2[5]	ms
Pushing figure				0.2		ppm/V
Fref buffer output level	V_{Fref}	Max. loading = 19pF	0.8[5]			$V_{p\text{-}p}$
Fref buffer output phase noise		10kHz offset Jitter noise		-140		dBc/Hz

[1, 2]: Tested at E-GSM Tx channel 0 and GSM850 Rx channel 190.
[3, 4]: Tested at PCS Tx channel 601 and DCS Rx channel 636.
[5]: Not subject to production test – verified by characterization and design.

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2.8 Bluetooth

2.8.1 Block Description

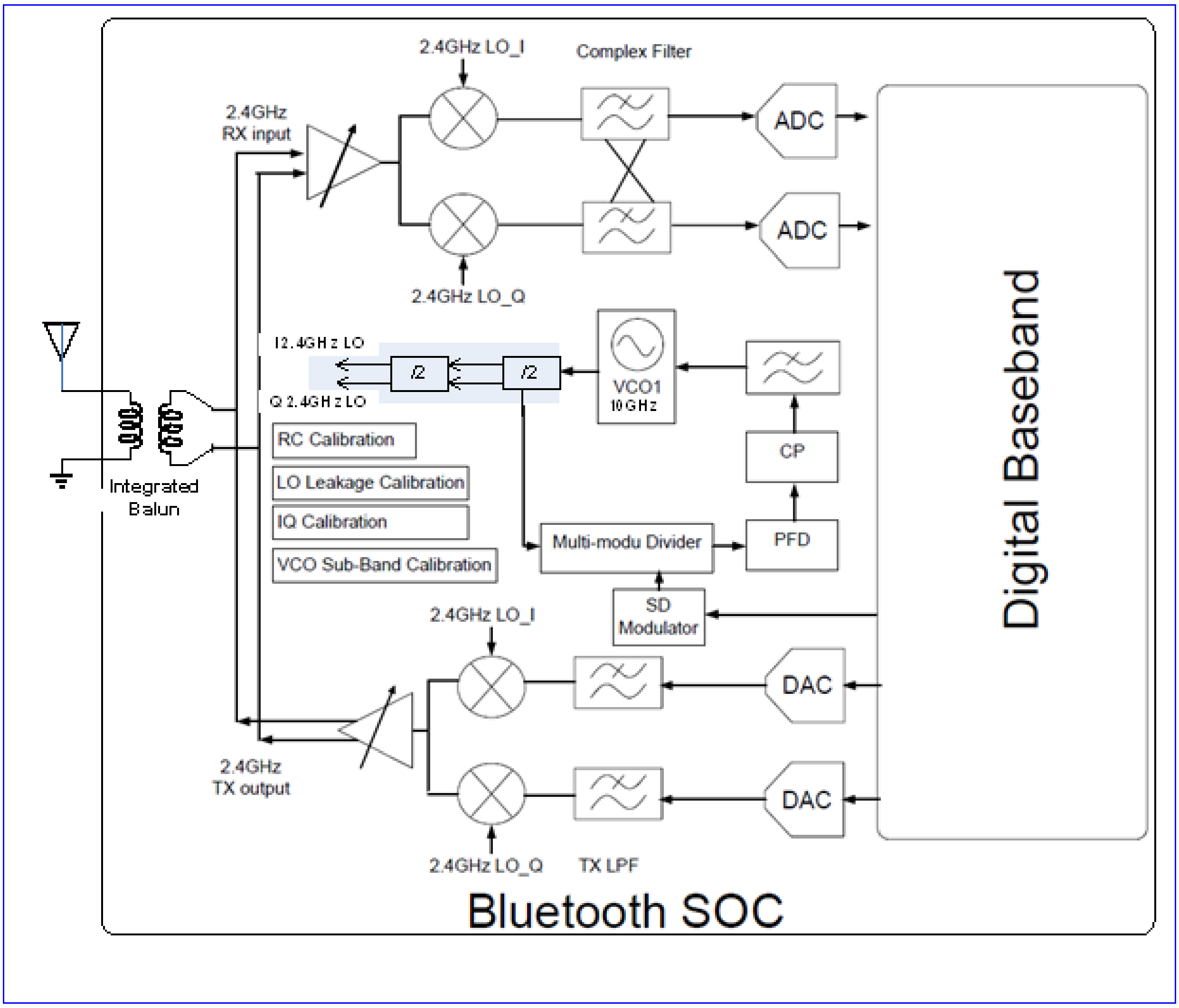

Figure 16. ***System diagram of Bluetooth RF transceiver***

The Bluetooth RF subsystem contains a fully integrated transceiver.

For TX path, the baseband transmit data are digitally modulated in the baseband processor then up-converted to 2.4GHz RF channels through the DA converter, filter, IQ up-converter and the power amplifier. The power amplifier is capable of transmitting 10dBm power for class-1.5 peration.

For RX path, MT6260A is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with the LO from the synthesizer, which supports different clock frequencies as the reference clock. The mixer output is then converted to digital signal and down-converted to baseband for demodulation. A fast AGC enables the effective discovery of device within the dynamic range of the receiver.

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MT6260A features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after system boot-up.

2.8.2 Functional Specifications

2.8.2.1 Basic Data Rate – Receiver Specifications

Table 40. Basic data rate – receiver specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	BER < 0.1%	-	-95	-	dBm
	Max. detectable input power	BER < 0.1%	-	0	-	dBm
	C/I co-channel selectivity	BER < 0.1%	-	4	-	dB
	C/I 1 MHz adj. channel selectivity	BER < 0.1%	-	-12	-	dB
	C/I 2 MHz adj. channel selectivity	BER < 0.1%	-	-47.5	-	dB
	C/I ≥ 3 MHz adj. channel selectivity	BER < 0.1%	-	-46	-	dB
	C/I image channel selectivity	BER < 0.1%	-	-24	-	dB
	C/I image 1 MHz adj. channel selectivity	BER < 0.1%	-	-45	-	dB
	Out-of-band blocking	30 to 2,000 MHz	-	-4	-	dBm
		2,000 to 2,399 MHz	-	-18	-	dBm
		2,498 to 3 000 MHz	-	-18	-	dBm
		3,000 MHz t 12 75 GHz	-	1	-	dBm
	Intermodulation		-	-22	-	dBm

2.8.2.2 Basic Data Rate – Transmitter Specification

Table 41. Basic data rate – transmitter specification

Symbol	Description	Condition	Min	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Maximum transmit power		-	9.5	-	dBm
	Gain step		-	4	-	dB
	Δf1avg (00001111)		140	158	175	kHz
	Δf2max (10101010)		115	130	-	kHz
	Δf1avg/Δf2avg		0.8	0.9	-	kHz
	Initial carrier frequency drift		-75	5	75	kHz
	Frequency drift	DH1	-25	9	25	kHz

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		DH3	-40	10	40	kHz
		DH5	-40	10	40	kHz
	Max. drift rate		-	100	400	Hz/µs
	BW_{20dB} of Tx output spectrum		-	920	1,000	kHz
	In-band spurious emission	±2 MHz offset	-	-38	-	dBm
		±3 MHz offset	-	-43	-	dBm
		> ±3 MHz offset	-	-43	-	dBm
	Out-of-band spurious emission	30 MHz to 1 GHz	-	-36	-	dBm
		1 to 12.75 GHz	-	-30	-	dBm
		1.8 to 1.9 GHz	-	-47	-	dBm
		5.15 to 5.3 GHz	-	-47	-	dBm

2.8.2.3 Enhanced Data Rate – Receiver Specifications

Table 42. Enhanced data rate – receiver specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	π/4 DQPSK, BER < 0.01%	-	-95	-	dBm
		8PSK, BER < 0.01%	-	-88	-	dBm
	Max. detectable input power	π/4 DQPSK, BER < 0.01%	-	-4.5	-	dBm
		8PSK, BER < 0.01%	-	-4.5	-	dBm
	C/I co-channel selectivity	π/4 DQPSK, BER < 0 01%	-	8	-	dB
		8PSK, BER < 0.01%	-	14.5	-	dB
	C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0 01%	-	-13	-	dB
		8PSK, BER < 0.01%	-	-7	-	dB
	C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-47.5	-	dB
		8PSK, BER < 0.01%	-	--41.5	-	dB
	C/I ≥ 3MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-48	-	dB
		8PSK, BER < 0.01%		44.5	-	dB
	C/I image channel selectivity	π/4 DQPSK, BER < 0.01%	-	30	-	dB
		8PSK, BER < 0.01%	-	23	-	dB
	C/I image 1 MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-47 5	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB

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2.8.2.4 Enhanced Data Rate – Transmitter Specifications

Table 43. Enhanced data rate – transmitter specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Max transmit power	π/4 DQPSK	-	6.5	-	dBm
		8PSK	-	6.5	-	dBm
	R lativ transmit power	π/4 DQPSK	-	-1.7	-	dB
		8PSK	-	-1.7	-	dB
	Freq. stability ω_0	π/4 DQPSK	-	1.5	-	kHz
		8PSK	-	1.5	-	kHz
	Freq. stability ω_1	π/4 DQPSK	-	3	-	kHz
		8PSK	-	3	-	kHz
	$\vert \omega_0+\omega_1 \vert$	π/4 DQPSK	-	2.8	-	kHz
		8PSK	-	2.8	-	kHz
	RMS DEVM	π/4 DQPSK	-	5.4	-	%
		8PSK	-	5.7	-	%
	99% DEVM	π/4 DQPSK	-	10	-	%
		8PSK	-	11	-	%
	Peak DEVM	π/4 DQPSK	-	18	-	%
		8PSK	-	18	-	%
	In-band spurious emission	π/4 DQPSK, ±1 MHz offset	-	-28	-	dBc
		8PSK, ±1 MHz off et	-	-28	-	dBc
		π/4 DQPSK, ±2 MHz offset	-	-25	-	dBm
		8PSK, ±2 MHz offset	-	-25	-	dBm
		π/4 DQPSK, ±3 MHz offset	-	-40.5	-	dBm
		8PSK, ±3 MHz offset	-	-40.5	-	dBm

Note: To meet this specification, use a front-end band-pass filter.

2.9 FM RF

2.9.1 Block Description

The connection between internal modules, as well as, external interfaces can be found n Figure 17. The FM receiver section incorporates the complete receiving path with wide tuning range. The FM baseband signal processor incorporates the digital demodulator and audio processing function which provides superior audio quality.

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FM contains completely integrated FM audio receiver functions (RDS/RBDS may also be supported depending on the model number). The integrated receiver enables superior sensitivity, ACI performance and FM audio performances with minimum external BOM.

The FM subsystem supports either high performance stereo analog line out or digital audio output(I2S).

For models supporting RDS/RBDS, large dedicated internal data buffers are allocated to reduce the frequency of the inter upt to the host, so that the receiving host can enter low power states efficiently.

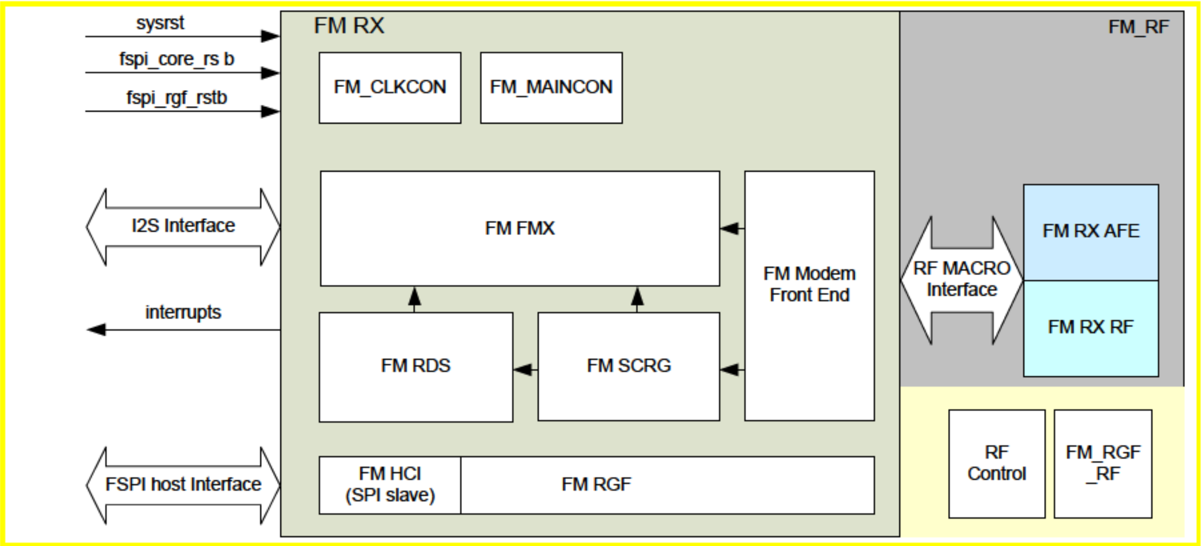

Figure 17. Block diagram of hardware top-level architecture

2.9.2 Functional Specifications

Table 1. FM receiver DC characteristics (TA=25°C, VDD=2.8V unless otherwise stated)

Operating mode	Current consumption	U it
Idle	5	μA
FM receiver	12	mA

Unless otherwise stated, all receiver characteristics are applicable to both long and short antenna ports when operated under the recommended operating conditions. Typical specifications are for channel 98.7 MHz, default register settings and under recommended operating conditions. The minimum and maximum specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

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Table 2. FM receiver AC characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Input frequency range		65		108	MHz
	Sensitivity (long antenna)[1,3]	(S+N)/N=26dB, unmatched		3		dBµVemf
		(S+N)/N = 26dB, matched		2		dBµVemf
	RDS sensitivity (long nten a)	Δf=2kHz,BLER<5%, unmatched		18		dBµVemf
	S nsitivity (short antenna)[1 3]	(S+N)/N=26dB, unmatched		3		dBµVemf
	RDS sensitivity (short antenna)	Δf=2kHz,BLER<5%, unmatched		18		dBµVemf
	LNA input resistance[4]			2.4k		Ohm
	LNA input capacitance[4]			8		pF
	AM suppression[1,4]	M = 0.3		58		dB
	Adjacent channel selectivity[1,4]	±200 kHz		53		dB
	Alternate channel selectivity[1,4]	±400 kHz		65		dB
	Spurious response rejection[4]	In-band		55		dB
	Maximum input level			117		dBµVemf
	Audio mono (S+N+D)/(N+D)[1,3,4]			60		dB
	Audio stereo (S+N+D)/(N+D)[2,3,4]			52		dB
	Audio stereo separation[4]	Δf = 22.5 kHz		45		dB
	Audio output load resistance	Single-ended at AFR/AFL outputs		10k		Ohm
	Audio output load capacitance	Single-ended at AFR/AFL outputs		12.5		pF
	Audio output voltage[1,4]	At AFR/AFL outputs		80		mVrms
	Audio output THD[1,4]			0.05	0.1	%
	Audio output frequency range	3dB corner frequency	30		15k	Hz

[1] Δf = 22.5kHz, fm = 1kHz, 50µs de-emphasis, mono, L = R

[2] Δf = 22.5kHz, fm = 1kHz, 50us de-emphasis, stereo

[3] A-weighting, BW = 300 Hz to 15 kHz

[4] Vin = 60dBµVemf

[5] Reference clock accuracy assumes ideal FM source. If the input FM source has less frequency error, then it is recommended to use a reference clock of accuracy within ±100ppm so as not to affect the channel scan quality.

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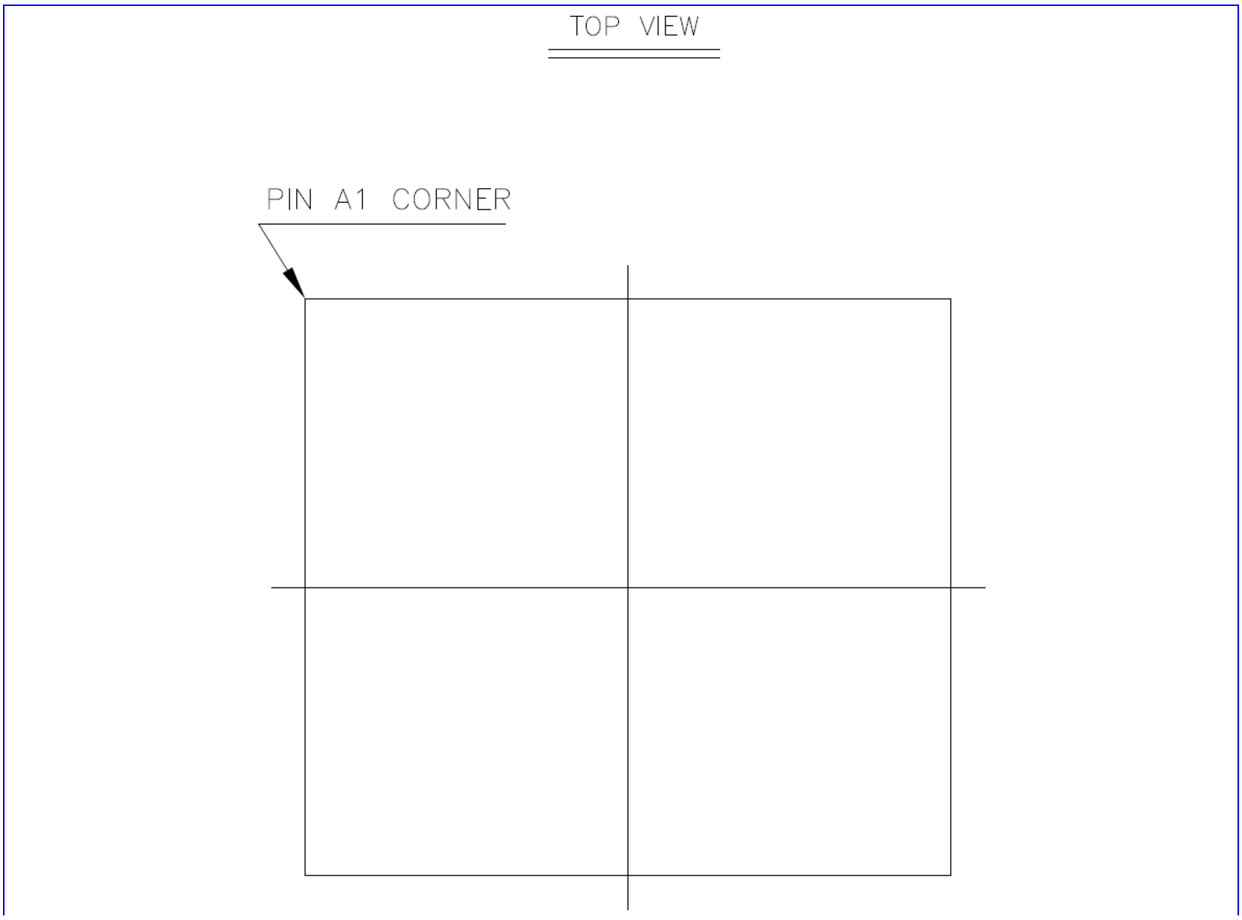
2.10 Package Information

2.10.1 Package Outlines



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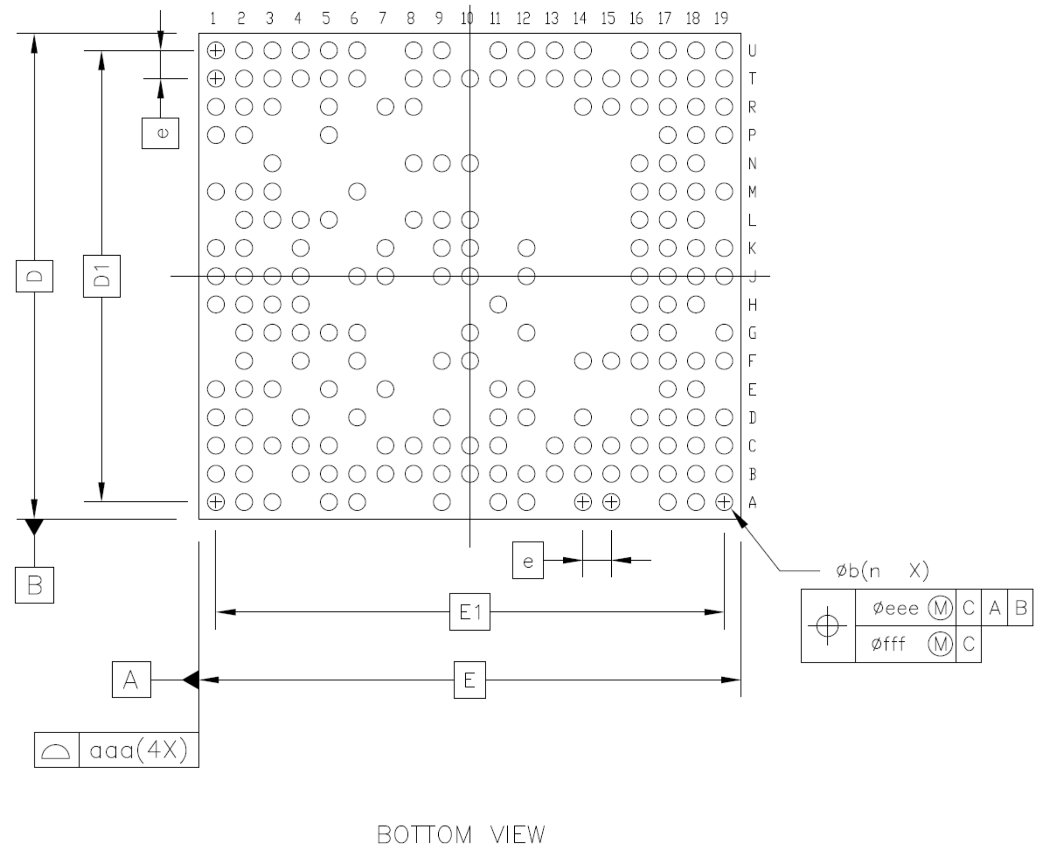

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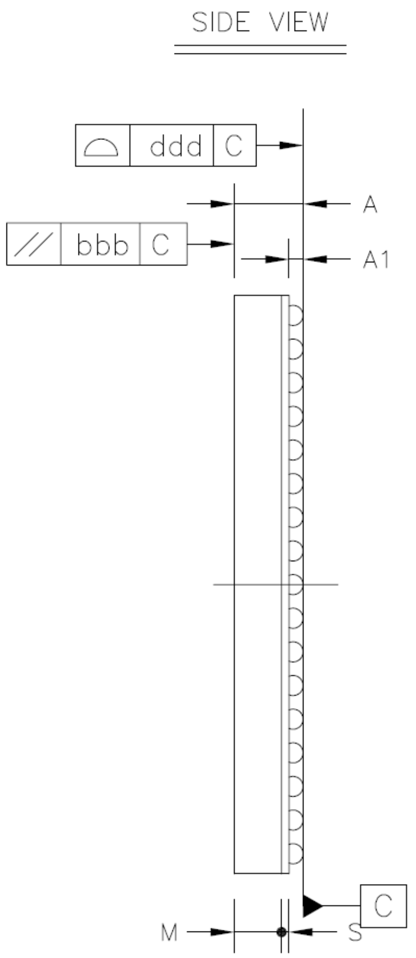

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		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			SBS TFBGA		
Body Size:	X	E	9.600		
	Y	D	8.600		
Ball Pitch :		e	0.500		
Total Thickness :		A	—	—	1.100
Mold Thickness :		M	0.700 Ref.		
Substrate Thickness :		S	0.110 Ref.		
Ball Diameter :			0.300		
Stand Off :		A1	0.160	—	0.260
Ball Width :		b	0.250	—	0.350
Package Edge Tolerance :		aaa	0.100		
Mold Flatness :		bbb	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.050		
Ball Count :		n	199		
Edge Ball Center to Center :	X	E1	9.000		
	Y	D1	8.000		

Figure 18. ***Outlines and dimension of TFBGA 9.6mm*8.6mm, 199-ball, 0.5 mm pitch package***

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2.10.2 Thermal Operating Specifications

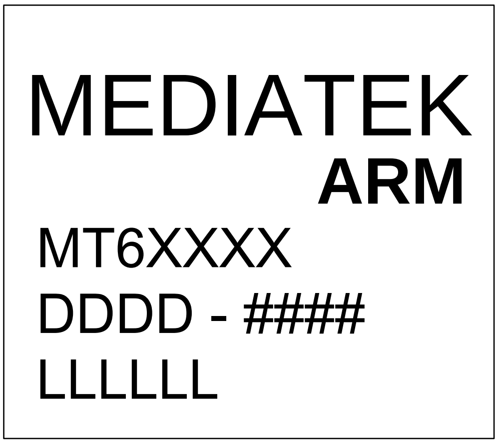
Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case	48	C/W	
	Maximum package temperature	65	Deg C	
	Maximum power dissipation	1.28	W	

2.10.3 Lead-free Packaging

MT6260A is provided in a lead-free package and meets RoHS requirements

2.11 Ordering Information

2.11.1 Top Marking Definition



MTXXXXXX Product No.
DDDD: Date Code
####: Subcontractor Code
LLLLLL: Die Lot No.

Figure 19. ***Mass production top marking of MT6260A***

Part number	Package	Description
MT6260A/A	TFBGA	8.6mm*9.6mm, 199 ball 0.5 mm pitch package, non-security versi n

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